Fully Integrated Single Photon Avalanche Diode Detector in Standard CMOS 0.18-μm Technology

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***Abstract*—Avalanche photodiodes (APDs) operating in Geiger mode can detect weak optical signals at high speed. The implementation of APD systems in a CMOS technology makes it possible to integrate the photodetector and its peripheral circuits on the same chip. In this paper, we have fabricated APDs of different sizes and their driving circuits in a commercial 0.18-μm CMOS technology. The APDs are theoretically analyzed, measured, and the results are interpreted. Excellent breakdown performance is measured for the 10 and 20 μm APDs at 10.2 V. The APD system is compared to the previous implementations in standard CMOS. Our APD has a 5.5% peak probability of detection of a photon at an excess bias of 2 V, and a 30 ns dead time, which is better than the previously reported results.**

***Index Terms*—Avalanche photodiodes (APDs), integrated photodetector, silicon avalanche photodiode (SAPD), silicon photodetector, single photon detectors.**

I. Introduction

VERY WEAK optical signals have to be measured in different fields of sciences including nuclear physics, chemistry, biology, and astronomy [1], [2]. For example, very low levels of fluorescence emission should be detected from the spots on a DNA microarray that corresponds to weakly expressed genes of the sample [3]. Detection of these light levels can be done using charge-coupled devices (CCDs) with ultralow-noise readout circuitry [4], [5], or modern CMOS photodetectors [6]–[8]. In these devices, the generated photocurrent is integrated in internal capacitors to convert the photocurrent to a voltage. Therefore, detecting lower levels of light with these devices requires longer integration times.

Applications like quantum cryptography [9], profilometry of remote objects [10], and fluorescence spectroscopy [11], however, require both high sensitivity and fast response of the photodetector. For example, photomultiplier tubes (PMTs) with microchannel plates are commonly used in fluorescence spectroscopy applications to detect single photons in picosecond–nanosecond regime [12], [13]. In terms of sensitivity and fast temporal response, PMTs are the best photodetectors available, and are widely used in applications such as fluorescence lifetime measurements. For the emerging miniaturized and portable applications, however, PMT-based photodetection systems have several significant disadvantages including: 1) requirement of high voltage ($\sim$1 KV or higher), which needs bulky specialized circuitry and power supplies; 2) use of glass vacuum tubes that are very fragile and large in size, which is not ideal for rugged and size sensitive medical and industrial applications; and 3) time-consuming individualized production/quality control with significantly high cost [14]–[16].

Avalanche photodiodes (APDs) operated in Geiger mode [17] are the semiconductor equivalent of PMTs. The APDs are used in discrete packages made with special processes, and are often connected to a detection and control electronic chip [18]. To increase the use of APD-based detector systems for biomedical applications, integration of the APD and peripheral circuitry on the same chip is highly desired [19].

Standard CMOS technology can be used to integrate the photodetector and driving circuits on the same chip. Such CMOS circuits are inexpensive and typically consume low power. Also, fast and compact digital circuit modules are available in CMOS. For imaging applications, the active pixel sensor (APS) structure is the most popular pixel configuration in CMOS. The APS consists of a photodiode, and reset, buffer, and select transistors. Recent APS circuits in CMOS technology have improved in resolution and sensitivity [20], [21]. However, the APS uses a photocurrent integration technique, so that it cannot offer both high speed and low light detection characteristics at the same time.

The fabrication of APDs in CMOS technology makes it possible to achieve the benefits of the APD as photodetector, and the necessary peripheral circuits on the same chip for an integrated system. However, APDs are difficult to make in CMOS technology, as they need special fabrication steps that might not be available in standard CMOS process. Nevertheless, significant advances have been reported by several groups [22]–[26]. In [22], results of a Geiger mode avalanche photodiode (GMAP) fabricated in 1.5-μm CMOS for use as a photoreceiver were reported. A data rate of 1 Gb/s in the optical data link was achieved from simulations in this work. In [23], several silicon avalanche photodiodes (SAPDs) were fabricated in 0.8-μm CMOS technology. The SAPDs had a 0.5 mm^2 area with a 400 pA/mm^2 measured dark current, but they were not operated in Geiger mode. In [24], the performance of a linear array of single photon avalanche diodes (SPADs) with passive quenching in 0.8-μm CMOS technology was reported. For the 5-μm APD, the dark count was 100 Hz and the dead time of the output was 1 μs. In [25], an SPAD with active quench and reset circuits in 0.8-μm

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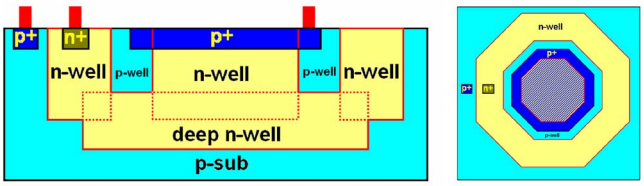


(a) (b)

Fig. 1. Layouts of our ADP. (a) Cross-sectional view. (b) Plan view. Putting an n-well inside a p^+ region creates the avalanche area and also the guard ring.

CMOS technology was described. A peak detection efficiency of 45% for a 10 V applied excess bias was reported. At this voltage, the dark count was 40 kcounts/s at room temperature. The overall size of the chip that operates a single 12-μm diameter APD was 1.1 mm $\times$ 2 mm. In [26], an SPAD array in 0.35-μm technology was described. The peak photon detection probability for this SPAD array was 5% for a 3 V excess bias, and the dead time was 40 ns.

In this paper, we have designed and fabricated an APD along with the driving circuitry in a standard 0.18-μm CMOS technology. In the next section, the structure of the APD and the schematic of its peripheral circuits will be introduced. Fabrication of the APDs is discussed in Section III. Then, in the measurements section, the APDs will be characterized, and results of the integrated detector and peripheral circuits are discussed. Our results are also compared with those for the previous implementations of APDs in CMOS. The conclusions of the work are given in Section V.

II. Designed APD

A regular p^+ n-well diode is fabricated in standard CMOS technology as a p^+ region implanted within an n-well region. In this diode, the breakdown current will not flow uniformly across the area of the p^+ region. The breakdown region of such diode will be at its edge (this will be discussed later in Section IV-A). This is due to the higher peak electric field caused by the narrower depletion region at the corners of the diode junction. As the reverse bias increases, electric field at the perimeter will reach the onset of avalanche first, and the current will flow there. In APDs, however, it is desired for the breakdown region to be spread over the area of the diode. We have made this possible by creating a p-type guard ring around the p^+ active area of the APD, as shown in Fig. 1. To create the guard ring, an n-well region is placed within the p^+ region, which is against the conventional rules of the standard CMOS. In our design, the width of the guard ring is 3 μm, with a depth of approximately 0.5 μm. The doping concentration of the p-well is in the range of 10^{17}cm^{-3} as compared to 10^{19} cm^{-3} for the p^+ region. It will be shown that the designed device has excellent avalanche characteristics. However, it should be noted that standard CMOS technology is targeted for digital and analog applications and not optical imaging devices. Most of our design parameters are not optimum, and are dictated by constraints of the fabrication technology. Fig. 2 shows the profile of the electric field created in our APD. The general neural simulation system (GENESIS) package is used to simulate some of the APD performance characteristics. The structure is produced with MDRAW (device editor and mesh generator application), and the electric field profile is obtained with device simulation for smart integrated systems (DESSIS). Fig. 2 shows that the peak electric field is spread under the active region of the APD, which is the p^+ n-well junction.

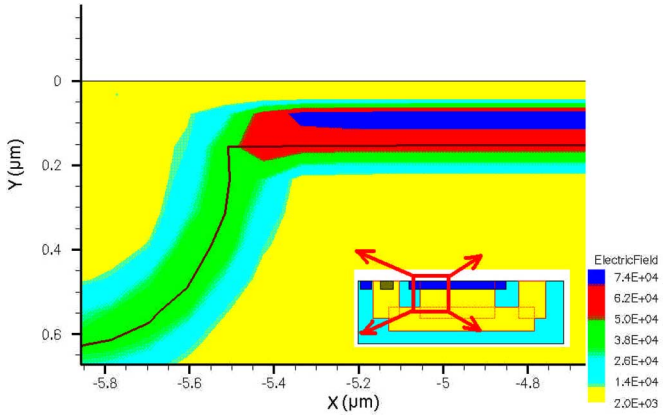
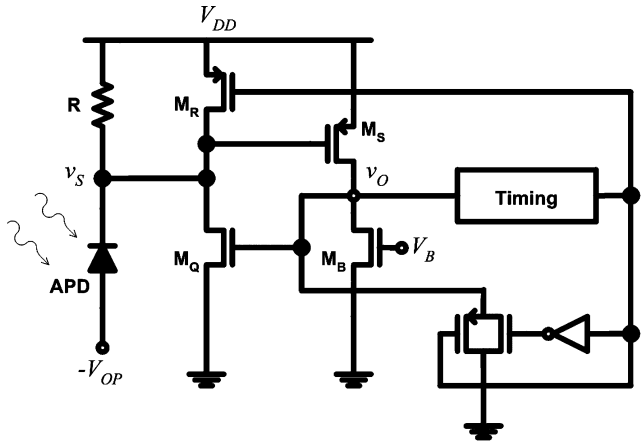
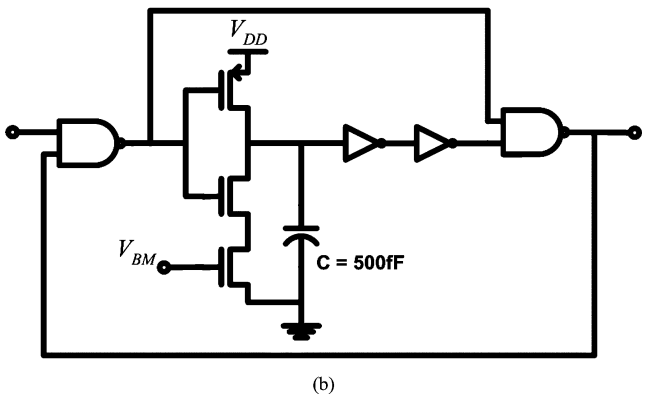


Fig. 2. Device simulation of the APD under reverse bias using the DESSIS tool. It shows that the maximum electric field will appear in the desired p^+ n-well junction.



(a)



(b)

Fig. 3. (a) Schematic of the APD circuit with active quench and active reset. The timing block consists of two monostables in series. (b) Simplified schematic of the monostable. Each monostable has a bias input that adjusts the width of the output pulse. The first monostable causes a delay and the second monostable dictate the width of the output of the timing block.

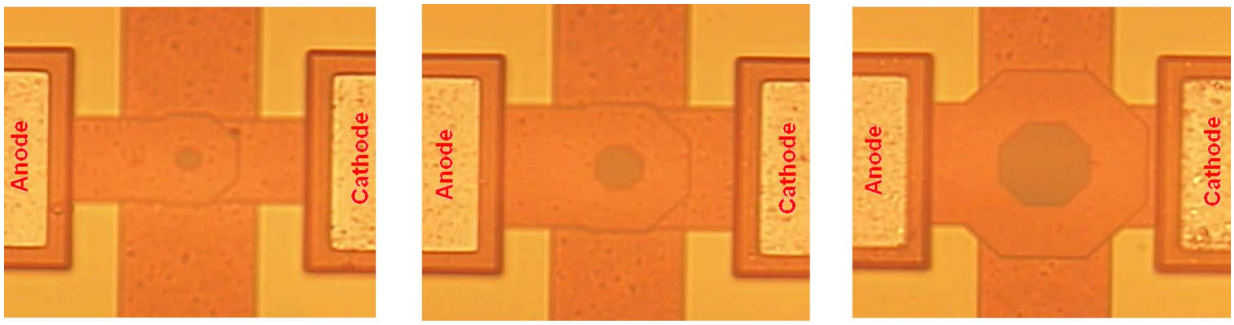


Fig. 4. Layouts of our APDs. (a) With 5-μm diameter. (b) With 10-μm diameter. (c) With 20-μm diameter. Design rules of the technology do not allow circular features. We have used 45° rotated lines to draw octagons, the closest shape that can be generated to circles.

Fig. 3(a) shows the schematic of APD and its associated peripheral circuits for operation in Geiger mode. When no current flows in the APD, its reverse bias equals to $(V_{\rm DD} + V_{\rm OP})$. This voltage is above the APD's breakdown voltage $V_{\rm BR}$. Several terms have been used in the literature for the difference between these voltage levels such as overvoltage, excess voltage, and excess bias. We will use the term excess bias in this paper. The value of the excess bias V_E is, then, given by

$$V_E = V_{\rm DD} + V_{\rm OP} - V_{\rm BR}. \quad (1)$$

An electron–hole pair can be generated in the depletion region of the APD, either by an incident photon or thermal generation. The electron and hole will, then, accelerate in the high electric field. They will collide with the lattice atoms, and release other carriers to start the avalanche process. This avalanche current builds up very fast. The current will flow in the quench resistor R, and cause the voltage at the sense node v_S to decrease. The quenching loop sense transistor M_S will sense this drop, and immediately turn ON the quench transistor M_Q to quickly bring the v_S down to zero. Now, the reverse bias applied to the APD is down to $V_{\rm OP}$, which is less than $V_{\rm BR}$. The avalanche process will stop and the current in the APD will immediately dissipate. The action performed by M_Q is called active quenching, and it causes the duration of the avalanche current flow in the APD to be short.

The sense node voltage is kept at zero for a hold-off time in order to reduce the probability that a subsequent after-pulse is triggered by the release of a trapped carrier. The hold-off time is controlled by a monostable in the timing block. At the end of the hold-off time, M_Q will be turned off and the reset transistor M_R will be turned on. Transistor M_R will bring v_S back to $V_{\rm DD}$ to make the APD ready for the next incoming photon. This is called active reset, and its duration is controlled by a second monostable in the timing block. At the end of reset time, M_R is turned off, and APD is ready to detect another photon.

The timing block in Fig. 3(a) consists of two monostables. The first one controls the quench time of the APD, and simply causes a delay between the time it senses the input and the time that it activates M_R. The second monostable controls the reset time, which is the duration of the output pulse that keeps M_R on. Both the monostables have a 500 fF internal capacitor and bias inputs that control the output pulse duration. Fig. 3(b) shows a simplified schematic of the monostable circuit used in this work [27]. Input $V_{\rm BM}$ is used to adjust the width of the output pulse of the monostable.

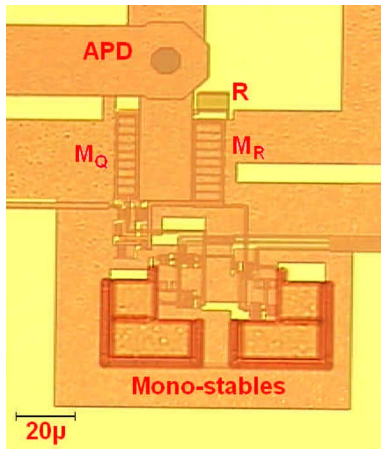


Fig. 5. Microphotograph of the layout of the APD with the peripheral circuits. A large part of the layout area is taken by the capacitors, which are seen as the two L-shaped features at the bottom of the microphotograph.

III. Fabrication

We have fabricated our APD in a 0.18-μm, single-poly, six-metal, salicide CMOS technology. We have fabricated APDs with three different diameters: 5, 10, and 20 μm. Fig. 4 shows the photomicrograph of these APDs with octagonal active regions. The guard rings of the APDs are shielded by metal layers. A circular shape is desired for APDs to reduce the possibility of corner breakdown. However, the layout rules for the technology do not allow for a circular shape; so, instead, the octagonal shape, which is closest to a circle that can be made, is designed. Measurements presented later show no corner breakdown of our APDs.

We have also fabricated the full circuit of Fig. 3, and a photomicrograph of its layout is shown in Fig. 5. Thick-oxide transistors are used so that 3 V for $V_{\rm DD}$ can be used instead of the 1.8 V that is typical of 0.18-μm CMOS technology. This higher $V_{\rm DD}$ will ensure that enough excess bias is applied to the APD when turned on, and that enough margin exists between

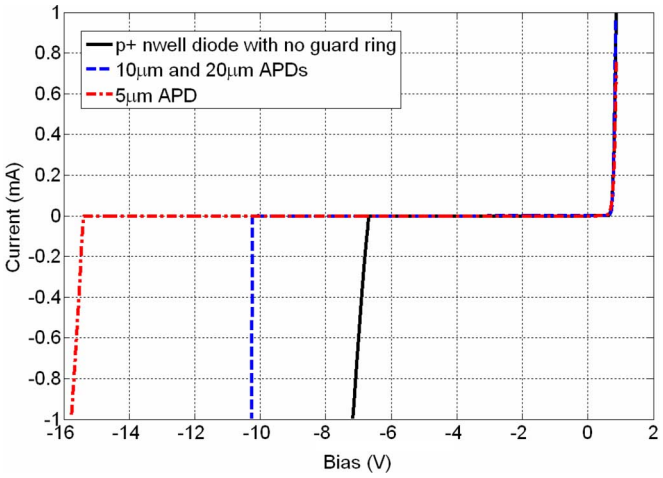


Fig. 6. Measured *I–V* profiles for different diodes. While a regular p^+ n-well diode shows a low breakdown voltage, our APDs with guard ring show an avalanche breakdown at 10.2 V. The 5 μm APD, however, has a high breakdown voltage.

$V_{\rm OP}$ and $V_{\rm BR}$. The APD can be displaced with respect to the peripheral circuit, to achieve a total pixel area of about 90 μm $\times$ 100 μm. Most of this area is taken by the capacitors of the monostables. The pixel reported in [10], which is a simple passive quenched APD with an inverter and a buffer, has a 1.1% fill factor. Our pixel, with active quench and active reset circuits, has the same fill factor. This has become possible by using a smaller scale CMOS technology.

IV. Measurements

Two types of measurements are performed. First, the APD is characterized. Then, the APDs with active quench and reset circuits are measured. These measurements and comparisons to theory are described after.

A. APD Characterization

The doping concentration levels in CMOS increase as the technology scales down, causing an increase in the peak electric field in the depletion region of the diodes. Therefore, the breakdown voltage decreases and the width of the depletion region will also decrease. Eventually, the doping levels can become high enough, resulting in very thin depletion region, and tunneling breakdown will replace the avalanche breakdown. Tunneling breakdown is known to happen for diodes with a breakdown voltage of about 7 V and lower.

For photon counting applications, we are interested in a diode that breaks down by avalanching. To our knowledge, all previous implementations of APDs in CMOS have used 0.35 μm or larger technology scales. Therefore, it is important to first investigate the breakdown mechanism of our APD made in this smaller scale CMOS technology. Fig. 6 shows the measured *I–V* curves for three different diodes that we have made in CMOS 0.18-μm technology. The measured curves are obtained with a 1 mA current compliance to protect the diodes. For a regular CMOS p^+ n-well diode that has no guard ring, that is, the p^+ region being surrounded in the n-well, as shown in Fig. 7(a), breakdown happens at approximately 6.7 V. It also does not have a sharp breakdown profile, indicating that edge breakdown is occurring. Our APD, with the structure shown in Fig. 7(b), has a very sharp breakdown at 10.2 V. The curve shows that the guard ring is effectively eliminating the edge breakdown of the p^+ n-well diode. The high breakdown voltage also suggests that the breakdown mechanism is avalanche, which will be proven later when the temperature-dependent analysis of the breakdown characteristics is described. The 10 and 20 μm APDs have similar breakdown behavior. However, interestingly, the 5 μm APD shows a different profile. Its breakdown starts at around 15.4 V with an edge breakdown like behavior. Fig. 7 illustrates the reason for the different breakdown characteristic of this diode. Fig. 7(b) shows the cross section of the 10-μm APD and the boundary of its depletion region. The effective area of the APD is reduced due to the depletion region around the guard ring. The area of the 10-μm APD is large enough to accommodate this depletion region such that the breakdown happens at the desired p^+ n-well junction. However, for the 5 μm APD shown in Fig. 7(c), the p-well regions get so close that the active area of the APD is almost fully depleted. Therefore, the p^+ n-well junction will no longer be working, and the APD performs like a p-well n-well diode. The breakdown will, now, happen at the sides of the p-well, as shown in Fig. 7(c). We have measured the breakdown voltage of a separate p-well n-well diode, made in CMOS 0.18-μm technology, to be 15.2 V. This confirms that the 5 μm APD operates like a p-well n-well diode.

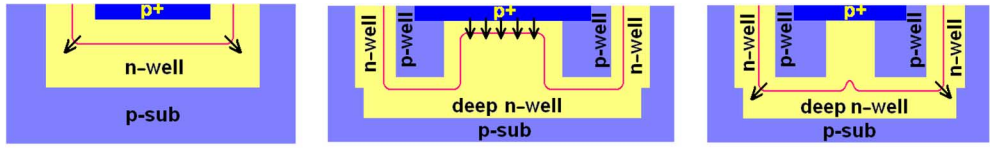
The breakdown voltage of the APD varies significantly with temperature. It was shown [28] that the breakdown voltage of silicon and other semiconductor APDs at temperature T can be described by

$$V_{\rm BR} = V_{\rm B0}[1 + \beta(T - T_0)] \tag{2}$$

where $V_{\rm B0}$ is the breakdown voltage at temperature T_0 (typically room temperature) and β is the temperature coefficient of the breakdown voltage. Previous studies [29], [30] show that the value of β is positive for diodes with avalanche breakdown and negative for diodes with tunneling breakdown. The theoretical derivation of β is presented in [31], and the theoretical values of β are compared with measured values for several diodes. A value of $7.2 \times 10^{-4}{}^{\circ}\mathrm{C}^{-1}$ for β is predicted in [31] for a diode with an avalanche breakdown voltage of about 10.2 V.

Fig. 8 shows how the measured breakdown voltage of our APDs varies with temperature. A breakdown voltage of 10.2 V is observed at room temperature (20 °C), and a value of $\beta = 7 \times 10^{-4}{}^{\circ}\mathrm{C}^{-1}$ is extracted for the thermal variation of the breakdown voltage. The positive value of β shows that the breakdown mechanism of our diode is indeed avalanche. The measured β is also in good agreement with the theoretical value [31].

A breakdown voltage of 23 V is reported for an APD fabricated in standard 0.35-μm CMOS [26]. We have measured a 10 V breakdown voltage for our APD made in 0.18-μm CMOS. Considering this trend, the breakdown voltage of APDs made in CMOS 0.13-μm or smaller will be low, and the breakdown mechanism will more likely be by tunneling. Thus, it can be expected that 0.18 or 0.13-μm will be the smallest geometry



(a) (b) (c)

Fig. 7. (a) Breakdown site of a regular p^+ n-well diode. (b) Breakdown site of 10-μm APD. (c) Breakdown site of 5-μm APD. The line shows the extent of the depletion region in the n-well.

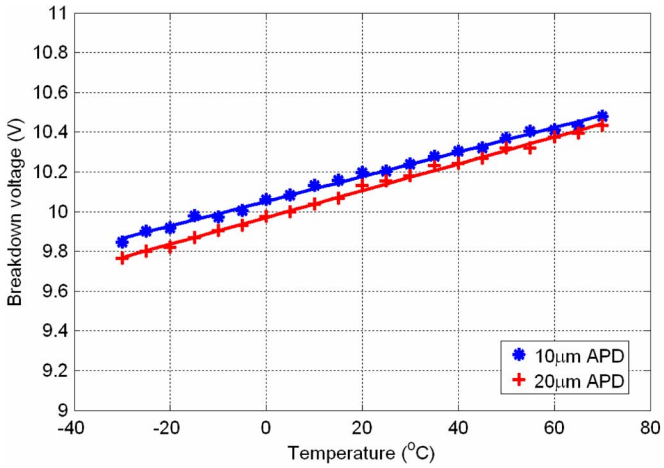


Fig. 8. Variation of the breakdown voltage of APDs with temperature. The rate of change is approximately 7 mV $^\circ$C^{-1} that results in $\beta \approx 7 \times 10^{-4}\,^\circ$C^{-1}.

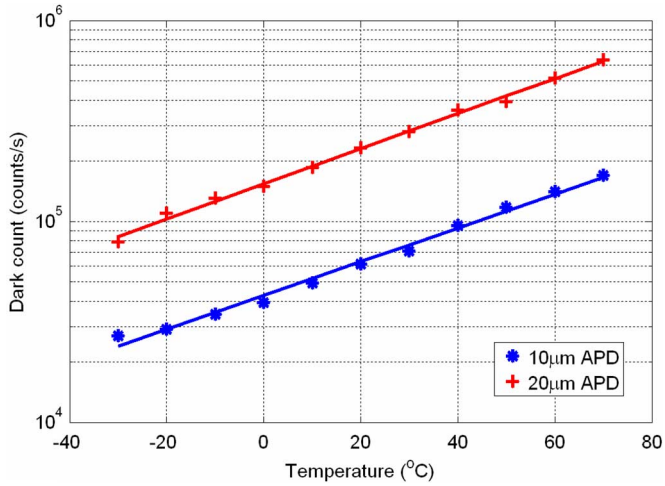


Fig. 9. Dark count versus temperature for an excess bias of 0.5 V. The dark count doubles approximately every 30°C.

CMOS technology for which an on chip GMAP fabrication is feasible.

It was mentioned earlier that an avalanche event can be triggered by either an incident photon, or a thermally generated electron–hole pair. The number of pulses per second that are generated by an APD in the absence of light is called dark count. Dark count sets the lower limit on the number of photons that can be detected per second. This is why APDs are cooled for low light level detection applications. The variation of the dark current of an APD with temperature follows the Meyer–Neldel law:

$$I_D = I_0 e^{-E_A/KT} \tag{3}$$

where E_A is the activation energy. Studying the activation energy can provide insight into the sources of the dark count. For diodes that the origin of dark carriers is pure thermal generation, the activation energy is normally approximately equal to half of the energy bandgap of the material. However, in diodes with a narrow depletion region, a dark carrier can be generated after tunneling into a midgap trap state. In the diodes that the generation of dark carriers is assisted by tunneling, the activation energy becomes smaller [32].

The measured dark counts of our 10 and 20 μm APDs are shown in Fig. 9. The variation of the dark count with temperature is measured for a fixed V_E of 0.5 V. The figure indicates that the dark count increases exponentially with temperature. The activation energy of the diode is $\sim$0.2 eV, which shows the dominance of the tunneling-assisted generation of the dark carriers. Note that this activation energy E_A was obtained from a plot of $\ln I_D$ against the inverse of the absolute temperature, according to (3). Also, our APD's dark count is relatively higher than the dark counts at 40 kHz reported in [25] or less than 1 kHz reported in [24] because of its lower breakdown voltage. The high doping concentration levels of 0.18-μm CMOS cause a narrow depletion region, resulting in a significant number of tunneling-induced dark carriers and increased dark count.

B. APD Full Circuit Performance

We have measured the performance of the APD with active reset and quench circuits. The dead time of an APD circuit is the time during which the APD cannot sense any incoming photon. It is the duration of the output pulse of the circuit that corresponds to a single incident photon (or thermally generated electron–hole pair). The dead time sets the upper limit on the number of photons that can be detected per second.

Dead time of an APD circuit can be analytically derived. Most of the dead time is taken by the active quench and active reset periods. When the avalanche process begins and the sense node voltage decreases by one threshold voltage of M_S, then the active quench loop turns the quench transistor on. Fig. 10(a) shows the approximate equivalent circuit during active quench. During this period, transistor M_Q brings v_S down to zero. The

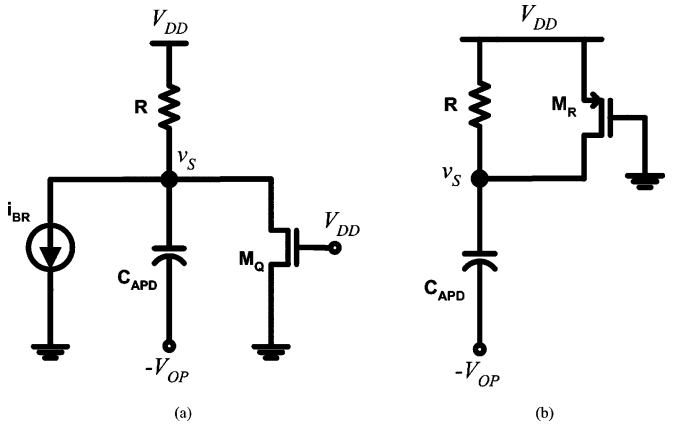


Fig. 10. Equivalent circuits used for analytical derivation of the sense node voltage. (a) During active quench. (b) During active reset.

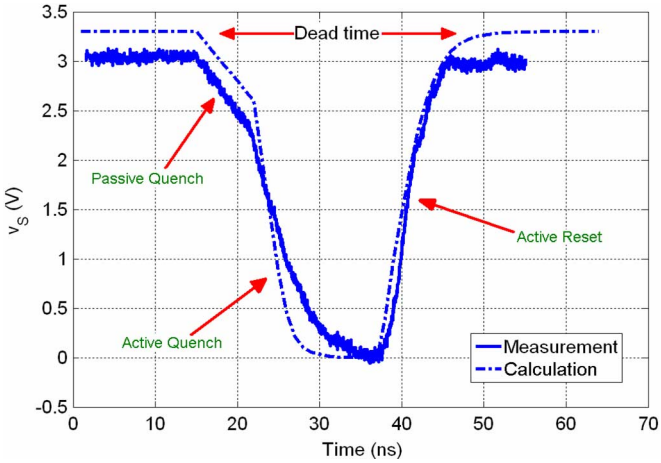


Fig. 11. Measured and simulated sense node voltage of the APD circuit. The dead time is about 30 ns.

relation governing the sense node voltage will, then, be

$$\frac{V_{\rm DD}-v_S(t)}{R}=C_{\rm APD}\frac{dv_S}{dt}+i_{\rm BR}+\mu_N C_{\rm ox}\frac{W_Q}{L_Q}\left[(V_{\rm DD}-V_{\rm TN})v_S(t)-\frac{v_S(t)^2}{2}\right] \quad (4)$$

with initial condition $v_S = V_{\rm DD} - V_{\rm TP}$. In (4), W_Q and L_Q are the width and length of the transistor M_Q, and $V_{\rm TN}$ is its threshold voltage. In our design, $W_Q/L_Q = 170$. The breakdown current of the APD is $i_{\rm BR}$, and $C_{\rm APD}$ is the capacitance of the APD measured to be 200 fF for the 10 μm APD at a reverse bias close to 10 V.

At the beginning of reset, the sense node voltage and the APD current are both zero. The transistor M_Q is turned off and M_R is turned on. Fig. 10(b) shows the circuit during reset. The equation governing the sense node voltage will, then, be

$$\frac{V_{\rm DD}-v_S(t)}{R}+\mu_P C_{\rm ox}\frac{W_R}{L_R}\left[(V_{\rm DD}-V_{\rm TP})[V_{\rm DD}-v_S(t)]-\frac{1}{2}[V_{\rm DD}-v_S(t)]^2\right]=C_{\rm APD}\frac{dv_S}{dt} \quad (5)$$

with initial value $v_S = 0$. In (5), W_R and L_R are the width and length of the transistor M_R, and $V_{\rm TP}$ is its threshold voltage. In our design, $W_R/L_R = 300$. For a period of time at the beginning of reset, the transistor M_R is in saturation. However, this time is very short as the sense node voltage will increase very fast and push the transistor M_Q into the linear regime of operation. Therefore, (5) is a good approximation for the whole reset period.

The output of the circuit of Fig. 3(a) has been measured to evaluate the response of the APD and peripheral circuits to incident photons. The output pad and measurement probes are connected to the node v_O in Fig. 3(a) to avoid loading the small capacitance of the sense node. Fig. 11 shows the variation of the sense node voltage of our circuit as a function of time. Since the start of avalanche in the APD, v_S will start to drop with passive quenching. It takes about 7 ns for v_S to reach a level that turns ON the quench loop. Fig. 11 also shows a quench time of about 15 ns and a reset time of about 8 ns. The times for active quench and active reset can be adjusted using the monostables of the timing block. These delays add to an overall dead time of about 30 ns. Previous implementations of APDs in CMOS have reported dead times of 60 ns [25] and 40 ns [10], [26]. These times are primarily affected by the capacitance of the APD including the capacitance of the guard ring, the size of the reset and quench transistors, and how well they can source or sink current. Fig. 11 also shows the calculated v_S using (4) and (5), which is in good agreement with the measured results.

Finally, the sensitivity and spectral response of our APD is investigated. The probability of detection of a photon (PDP) indicates the percentage of incoming photons that trigger a pulse in the output of the APD circuit. The PDP is measured by evaluating the number of photons incident on the APD, and counting the number of pulses in its output. The rate of the incoming photons is evaluated based on the power of the incident light at a certain wavelength. The number of pulses generated by the APD is measured in a fixed time interval several times, and then, averaged. Measurements are done using a stable wide-spectrum xenon lamp connected to an integrating sphere through bandpass filters and attenuators to adjust the wavelength and flux of the incident photons on the APD. Measurements are performed on a vibration isolation optical table. Measurements are repeated in dark, and the dark count is subtracted from the count of the output pulses of the APD at each measurement point. Fig. 12 shows the measured PDP as a function of the wavelength of the incoming light at different levels of V_E for the 10-μm APD.

The width of the depletion region and the strength of the electric field increase in an APD by applying higher V_E. This will make it easier for an electron–hole pair to start the avalanche breakdown. This is why PDP increases with V_E, as shown in Fig. 12. However, increasing V_E will also increase the dark count and noise of the APD. Also, in practice, when the APD is implemented in CMOS along with the active quench and reset circuits, V_E cannot be greater than $V_{\rm DD}$. This is according to (1) and the fact that $V_{\rm OP} < V_{\rm BR}$. Our APD shows a maximum PDP of about 5.5% for a V_E of 2 V. The PDP will improve with

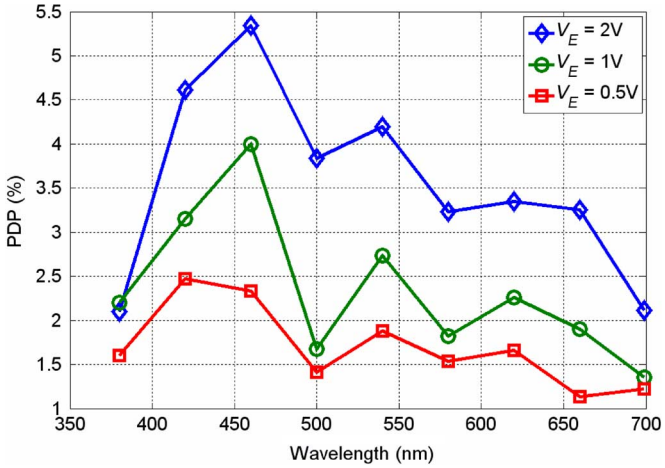


Fig. 12. Probability of detection of photons for different wavelengths. Increasing the excess bias will increase the probability of detection. Oscillations in the curves are due to the several dielectric layers of CMOS on top of the APD.

increasing excess bias, as reported in some previous publications. For example, in [26], a peak PDP of 5% for a V_E of 3 V was reported. In [10], the PDP was in 20% range for a V_E of 5 V, and in [25], the peak PDP was 45% for a V_E of 10 V. Note that the PDP can be further improved in our device by removing the passivation layer from the surface of the chip.

V. Conclusion

In this paper, single photon APDs, along with their peripheral circuitry, were integrated in a standard 0.18-μm CMOS technology. These APDs exhibited good avalanche breakdown characteristics. We expect that it will not be possible to make APDs with much smaller scale CMOS technologies, as the breakdown mechanism will switch to tunneling. Also, active quench and reset circuits have been successfully implemented and measured. Our integrated APD and peripheral circuits had a measured dead time of about 30 ns and a PDP of about 5.5% at an excess bias of 2 V—results that are comparable or better than the best published results to date. Fabrication of APDs in 0.18-μm technology improves the fill factor and increases the speed of the pixel. There is also a limit on how small the APD can be made when a standard CMOS technology is used. This is because of the interference of the depletion region of the guard ring with the APD effective sensing area.

References

[1] S. A. Soper, J. H. Flanagan, B. L. Legendre, D. C. Williams, and R. P. Hammer, "Near-infrared, laser-induced fluorescence detection for DNA sequencing applications," *IEEE J. Sel. Topics Quantum Electron.*, vol. 2, no. 4, pp. 1129–1139, Dec. 1996.

[2] N. S. Nightingale, "A new silicon avalanche photodiode photon counting detector module for astronomy," *Exp. Astron.*, vol. 1, pp. 407–422, 1991.

[3] J. Wang, "Survey and summary: From DNA biosensors to gene chips," *Nucleic Acids Res.*, vol. 28, no. 16, pp. 3011–3016, Aug. 2000.

[4] B. E. Bruke, R. K. Reich, J. A. Gregory, W. H. McGonagle, A. M. Waxman, E. D. Savoye, and B. B. Kosicki, "640 × 480 back-illuminated CCD imager with improved blooming control for night vision," in *IEDM Tech. Dig.*, Dec. 1998, pp. 33–36.

[5] S. Adachi, H. Simada, H. Gotoh, and K. Mizobuchi, "A novel lateral overflow drain technology for high quantum efficiency CCD imagers," in *IEDM Tech. Dig.*, Dec. 2000, pp. 693–696.

[6] T. Watabe, M. Goto, H. Ohtake, H. Maruyama, M. Abe, K. Tanioka, and N. Egami, "New signal readout method for ultrahigh-sensitivity CMOS image sensor," *IEEE Trans. Electron Devices*, vol. 50, no. 1, pp. 63–69, Jan. 2003.

[7] T. H. Hsu, Y. K. Fang, D. N. Yaung, J. S. Lin, S. G. Wuu, H. C Chien, C. H. Tseng, C. S. Wang, S. F. Chen, C. Y. Lin, C. S. Lin, and T. H. Chou, "An effective method to improve the sensitivity of deep sub-micrometer CMOS image sensor," *IEEE Electron Device Lett.*, vol. 26, no. 8, pp. 547–549, Aug. 2005.

[8] N. Faramarzpour, M. J. Deen, and S. Shirani, "Signal and noise modeling and analysis of complementary metal-oxide semiconductor active pixel sensors," *J. Vac. Sci. Technol. A, Vac. Surf. Films*, vol. 24, no. 3, pp. 879–882, 2006.

[9] K. J. Gordon, V. Fernandez, P. D. Townsend, and G. S. Buller, "A short wavelength gigahertz clocked fiber optic quantum key distribution system," *IEEE J. Quantum Electron.*, vol. 40, no. 7, pp. 900–908, Jul. 2004.

[10] C. Niclass, A. Rochas, P. A. Besse, and E. Charbon, "Design and characterization of a CMOS 3D image sensor based on single photon avalanche diodes," *IEEE J. Solid-State Circuits*, vol. 40, no. 11, pp. 1847–1854, Nov. 2005.

[11] H. K. Ki, C. Buehler, K. Bahlmann, and P. T. C. So, "Usage of multi-anode PMT on the multi-photon fluorescence spectroscopy and video rate microscopy," in *Proc. 24th EMBS/BMES*, Oct. 23–26, 2002, vol. 2, p. 1206.

[12] M. Kfouri, O. Marinov, P. Quevedo, N. Faramarzpour, S. Shirani, L. W.-C. Liu, Q. Fang, and M. J. Deen, "Towards a miniaturized wireless fluorescence-based diagnostic imaging system," *IEEE J. Sel. Topics Quantum Electron. (Special Issue on Biophotonics)*, vol. 14, no. 1, p. 9, Jan./Feb. 2008.

[13] Q. Fang, T. Papaioannou, J. A. Jo, R. Vaitha, K. Shastry, and L. Marcu, "Time-domain laser-induced fluorescence spectroscopy apparatus for clinical diagnostics," *Rev. Sci. Inst.*, vol. 75, no. 1, pp. 151–162, 2004.

[14] *Photomultiplier Tubes: Basics and Applications*, 3rd ed. Hamamatsu Photonics, Hamamatsu City, Japan, 2006.

[15] S. Mazeres, V. Borrel, C. Magenc, J. L. Courrech, and R. Bazer-Bachi, "APD detectors for biological fluorescence spectroscopy," *Nuclear Inst. Methods Phys. Res. A*, vol. 567, no. 1, pp. 255–259, 2006.

[16] M. A. Khan, M. Shatalov, H. P. Maruska, H. M. Wang, and E. Kuokstis, "III-nitride UV devices," *Jpn. J. Appl. Phys.*, vol. 44, pp. 7191–7206, 2005.

[17] J. C. Jackson, A. P. Morrison, D. Phelan, and A. Mathewson, "A novel silicon Geiger-mode avalanche photodiode," in *IEDM Tech. Dig.*, Dec. 2002, pp. 797–800.

[18] F. Zappa, A. Lotito, and S. Tisa, "Photon-counting chip for avalanche detectors," *IEEE Photon. Technol. Lett.*, vol. 17, no. 1, pp. 184–186, Jan. 2005.

[19] B. F. Aull, A. H. Loomis, J. A. Gregory, and D. J. Young, "Geiger-mode avalanche photodiode arrays integrated with CMOS timing circuits," in *Proc. Device Res. Conf. Dig.*, Jun. 1998, vol. 56, pp. 58–59.

[20] I. Takayanagi, M. Shirakawa, K. Mitani, M. Suqawara, S. Iversen, J. Moholt, J. Nakamura, and E. R. Fossum, "A 1.25-inch 60-frames/s 8.3M-pixel digital-output CMOS image sensor," *IEEE J. Solid-State Circuits*, vol. 40, no. 11, pp. 2305–2314, Nov. 2005.

[21] N. Faramarzpour, M. J. Deen, and S. Shirani, "An approach to improve the signal-to-noise ratio of active pixel sensor for low-light-level applications," *IEEE Trans. Electron Devices*, vol. 53, no. 9, pp. 2384–2391, Sep. 2006.

[22] A. M. Moloney, A. P. Morrison, J. C. Jackson, A. Mathewson, and P. J. Murphy, "Geiger-mode avalanche photodiode with CMOS transimpedance amplifier receiver for optical data link applications," in *Proc. IT&T. Conf. Transmiss. Tech.*, Oct. 2002, pp. 251–257.

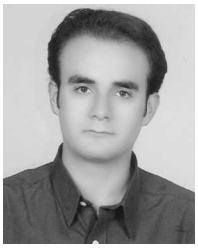
[23] A. Rochas, A. R. Pauchard, P. A. Besse, D. Pantic, A. Prijic, and R. S. Popovic, "Low-noise silicon avalanche photodiodes fabricated in conventional CMOS technologies," *IEEE Trans. Electron Devices*, vol. 49, no. 3, pp. 387–394, Mar. 2002.

[24] L. Pancheri and G. F. D. Betta, "CMOS distance sensor based on single photon avalanche diode," *Res. Microelectron. Electron.*, vol. 2, pp. 103–106, Jul. 2005.

[25] S. Tisa, F. Zappa, and I. Labanca, "On-chip detection and counting of single-photons," in *IEDM Tech. Dig.*, Dec. 5–7, 2005, pp. 815–818.

[26] C. Niclass, M. Sergio, and E. Charbon, "A single photon avalanche diode array fabricated on deep-submicron CMOS technology," in *Proc. Des. Autom. Test Eur.*, Munich, Mar. 2006, pp. 81–86.

[27] D. Cronin, A. M. Moloney, and A. P. Morrison, "Simulated monolithically integrated single photon counter," in *High Freq. Postgraduate Student Colloq.*, Manchester, Sep. 6–7, 2004, pp. 9–14.
[28] K. G. McKay, "Avalanche breakdown in silicon," *Phys. Rev.*, vol. 94, no. 4, pp. 877–884, May 1954.
[29] C. L. F. Ma, M. J. Deen, L. E. Tarof, and J. C. H. Yu, "Temperature dependence of breakdown voltages in separate absorption, grading, charge and multiplication InP/InGaAs avalanche photodiodes," *IEEE Trans. Electron Devices*, vol. 42, no. 5, pp. 810–818, May 1995.
[30] C. L. F. Ma, M. J. Deen, and L. Tarof, "Characterization and modelling of SAGCM InP/InGaAs avalanche photodiodes for multigigabit optical fiber communications," in *Advances in Imaging and Electron Physics,* vol. 99, P. Hawkes, Ed. New York, NY: Academic, 1998, pp. 65–170.
[31] M. S. Tyagi, "Zener and avalanche breakdown in silicon alloyed p-n junctions," *Solid-state Electron.*, vol. 11, pp. 99–128, Jan. 1968.
[32] M. A. Itzler, R. Ben-Michael, C. F. Hsu, K. Slomkowski, A. Tosi, S. Cova, F. Zappa, and R. Ispasoiu, "Single photon avalanche diodes (SPADs) for 1.5 μm photon counting applications," *J. Modern Opt.*, vol. 54, no. 2–3, pp. 283–304, Jan. 2007.



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