CMOS-Based Active Pixel for Low-Light-Level Detection: Analysis and Measurements

Naser Faramarzpour, *Student Member, IEEE*, M. Jamal Deen, *Fellow, IEEE*, Shahram Shirani, *Senior Member, IEEE*, Qiyin Fang, *Member, IEEE*, Louis W. C. Liu, Fernando de Souza Campos, and Jacobus W. Swart, *Senior Member, IEEE*

***Abstract*—An analysis of the active pixel sensor (APS), considering the doping profiles of the photodiode in an APS fabricated in a 0.18 μm standard CMOS technology, is presented. A simple and accurate model for the junction capacitance of the photodiode is proposed. An analytic expression for the output voltage of the APS obtained with this capacitance model is in good agreement with measurements and is more accurate than the models used previously. A different mode of operation for the APS based on the dc level of the output is suggested. This new mode has better low-light-level sensitivity than the conventional APS operating mode, and it has a slower temporal response to the change of the incident light power. At 1 μW/cm^2 and lower levels of light, the measured signal-to-noise ratio (SNR) of this new mode is more than 10 dB higher than the SNR of previously reported APS circuits. Also, with an output SNR of about 10 dB, the proposed dc level is capable of detecting light powers as low as 20 nW/cm^2, which is about 30 times lower than the light power detected in recent reports by other groups.**

***Index Terms*—Active pixel sensor (APS), capacitance–voltage (C–V) profile, CMOS photodetector, high-sensitivity photodetector, low-level light detection, silicon photodetector.**

I. Introduction

PHOTODETECTION systems are now being used in new applications in medicine, bio-molecular sciences, environmental monitoring, and chemistry experiments [1]–[3]. In many of these applications, the level of light that should be detected is very low, in the order of microwatts per square centimeter and less [4]. Many photodetector structures are not able to detect such low light intensities. The reason is the low signal-to-noise ratio (SNR) of these detectors at low levels of light. This deficiency of the detectors is compensated, for example, by increasing the level of light illuminating the biological sample under test. However, these high intensities can result in impaired cellular reproduction, formation of giant cells, oxidative stress and apoptosis-like cell death [5]. In some other applications such as fluorescence imaging, it will reduce the lifetime of the fluorophores [6], [7].

Photodetectors manufactured in CMOS technology are currently used in some biomedical applications such as chemical sensing systems and fluorescence imaging [8]–[10]. An important advantage for CMOS-based photodetectors is that the technology is cheap and it can be used to integrate processing and control circuitry on the same chip with the detector [11]. The active pixel sensor (APS) is the most commonly used structure for CMOS photodetector arrays. APS offers high fill-factor and wide dynamic range. These detectors are, however, noisy and do not have good performances at lower levels of light, unless they are operated with impractically long integration times [12].

For low-light-level applications, other photodetectors such as photomultiplier tubes (PMTs) or avalanche photodiodes (APDs), which have internal mechanisms for the amplification of light [13], are currently used. However, these photodetectors are not easy to integrate, and their operation typically requires high voltage levels. Charge-coupled devices (CCDs) are used for low-light-level sensing applications, as they have better noise performance than CMOS-based photosensors [14]. These CCD detectors, however, are expensive and consume high power. Also, CCDs have to be fabricated by special processes, and cannot easily be integrated with other circuitry. This is against the existing trend of integrating optical detection systems as much as possible.

In a previous work, we developed the theory of how the APS can be operated in a different mode and achieve better sensitivity at lower levels of light [15]. In this paper, we have expanded the analysis of the APS by measuring the capacitance–voltage (C–V) profile of the photodiode. We fabricated an APS in CMOS 0.18 μm technology, and operated it in the proposed mode. Our measurements verified that the pixel offers higher sensitivity at lower levels of light. It can detect light with at least two orders of magnitude lower intensity than the regular APS.

II. Theory

The photocurrent in a conventional APS is integrated in the capacitance of the photodiode. This capacitance is considered constant in many of the APS analyses reported [16]–[18]. The capacitance of the p-n junction, however, varies with voltage.

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N. Faramarzpour, M. J. Deen, and S. Shirani are with the Department of Electrical and Computer Engineering, McMaster University, Hamilton, ON L8S 4L8, Canada (e-mail: faraman@mcmaster.ca; jamal@mcmaster.ca; shirani@mail.ece.mcmaster.ca).

Q. Fang is with the Department of Engineering Physics, McMaster University, Hamilton, ON L8S 4L8, Canada (e-mail: qfang@mcmaster.ca).

L. W. C. Liu is with the Department of Medicine, University of Toronto, Toronto, ON M5S 3G4, Canada (e-mail: louis.liu@uhn.on.ca).

F. de Souza Campos is with the University of the State of São Paulo, Bauru, SP 17033-360, Brazil (e-mail: fcampos@feb.unesp.br).

J. W. Swart is with CenPRA–Tecnologia de Informação, Centro de Pesquisa Renato Archer, Rod. Dom Pedro I, Campinas, SP-CEP 13069-901, Brazil (e-mail: jacobus.swart@cenpra.gov.br).

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We will show that considering this variation greatly affects the result of the analysis of the APS. This variable capacitance was considered in [30], however, an abrupt junction model was used. We will show that fixed capacitance, or abrupt junction models do not provide good accuracy for the APS analysis. Our model for the capacitance of the photodiode will be presented, and then its effect on the analysis of APS will be shown.

A. Analysis of the APS During Integration

In a modern standard CMOS technology, n+ and p+ regions, wells, and channel profiles are made by the ion-implantation method. Ion-implantation offers good control over the number of impurities and their profile. Junctions produced with this method can be well controlled. The doping profile of implanted impurities has approximately a Gaussian distribution [19]

$$N(x) = \frac{\Phi}{\sqrt{2\pi}\Delta R_p} e^{-(x-R_p)^2/2\Delta R_p^2} \tag{1}$$

where Φ is related to the doping dose, R_p is the projection range, and ΔR_p is the straggle of the implanted species. Assuming $N(0) = A$ and $|x| \ll R_p$, then (1) can be approximated as

$$N(x) \approx Ae^{x/\beta} \tag{2}$$

where A and β are defined as

$$A = \frac{\Phi}{\sqrt{2\pi}\Delta R_p} e^{-R_p^2/2\Delta R_p^2} \tag{3}$$

and

$$\beta = \frac{\Delta R_p^2}{R_p}. \tag{4}$$

Equation (2) indicates that if the junction is a few standard deviations away from the range of the implantation, which is usually the case in CMOS technology, then the doping profiles at the junction can be approximated with exponential functions. In deep submicrometer technologies, extremely shallow implanted regions are desired. This calls for a reduction of the thermal budget of the process and creation of as-implanted profiles. Long channeling tails that would thermally be removed now become significant. This causes some deviation from the profile of (1), by reducing the slope of the deeper side of the implanted profile in the semilogarithmic plot [20], [21]. The profile in the semilogarithmic plot, however, stays approximately linear at a few straggles away from the range of the implantation. Thus, the exponential approximation of (2) remains valid for such processes, provided adjustments of the parameters defined in (3) and (4) are made.

For a p-n junction with exponential doping profiles as shown in Fig. 1, the voltage drop across the depletion region and the static charge in the depletion region, can be calculated, given the boundaries of the depletion region. Parameters w_n and w_p, in Fig. 1, indicate the depth of depletion of the n and p sides,

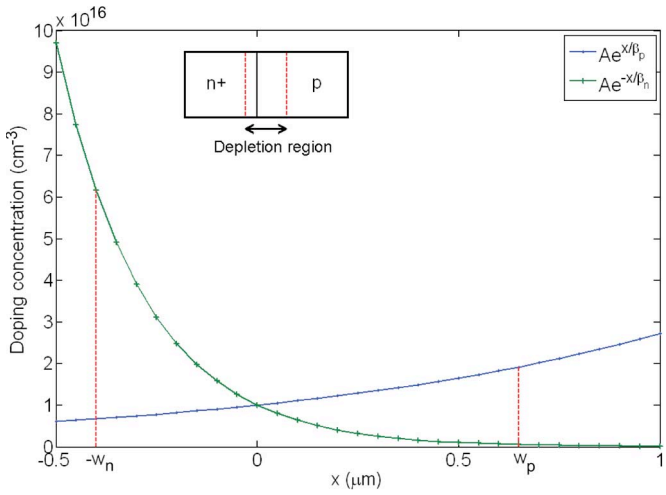


Fig. 1. Doping profiles at the junction between two ion-implanted regions. Profiles are close to exponential at the junction. w_n and w_p are boundaries of the depletion region.

respectively. Assuming that the n side is more highly doped than the p side, that is $\beta_n \ll \beta_p$, then $w_n \ll w_p$ and we get

$$V = \frac{qA\beta_p}{\varepsilon}(\beta_p - w_p)e^{w_p/\beta_p} \tag{5}$$

and

$$Q = qA\beta_p(e^{w_p/\beta_p} - 1) \tag{6}$$

where Q is the charge per unit area. The parameter w_p should be eliminated from (5) and (6), and $dQ/dV|_\nu$ should be calculated as the voltage-varying capacitance of the junction. A closed form equation for C per unit area, given ν, can be derived from (5) and (6) using a Lambert W function

$$C(\nu) = \frac{\varepsilon}{\beta_p}\left[1 + W\left(\frac{\varepsilon\nu}{\beta_p^2 qAe}\right)\right]^{-1}. \tag{7}$$

Note that the Lambert W function is the inverse of the function $f(W) = We^W$ [22], [23].

Equation (7) is the exact equation for the C–V characteristic of an exponential junction. However, it does not have a simple form for numerical evaluations and is difficult to be employed in the analysis. A $\nu^{-1/m}$ characteristic is traditionally assumed for the C–V relation of a p-n junction [12], [24]

$$C(\nu) = C_0 \sqrt[m]{\frac{\nu_0 + \varphi}{\nu + \varphi}} \tag{8}$$

where φ is the built-in potential of the junction, and ν_0 and C_0 are the values of photodiode voltage and capacitance at the beginning of integration. Trying to fit (8) to (7), we found that $m = 4$ is the optimum choice. Note that $m = 2$ corresponds to an abrupt junction, and $m = 3$ to a linear junction. Thus, $m = 4$ can be a good approximation for an exponential junction.

We measured the C–V characteristic of photodiodes fabricated in a commercial 0.18 μm technology to verify the above estimation of m. Measurements are done on 72 μm^2

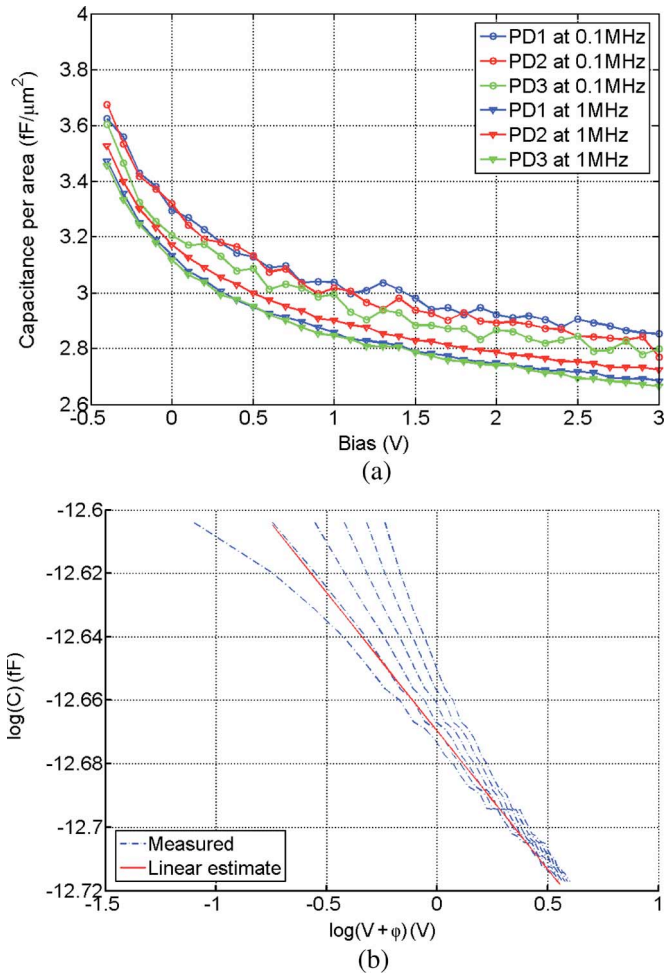


Fig. 2. (a) Measured C–V characteristics and (b) logarithm of capacitance versus voltage for different values of φ. The value of φ, which produces a straight line, is closest to the built-in potential of the junction.

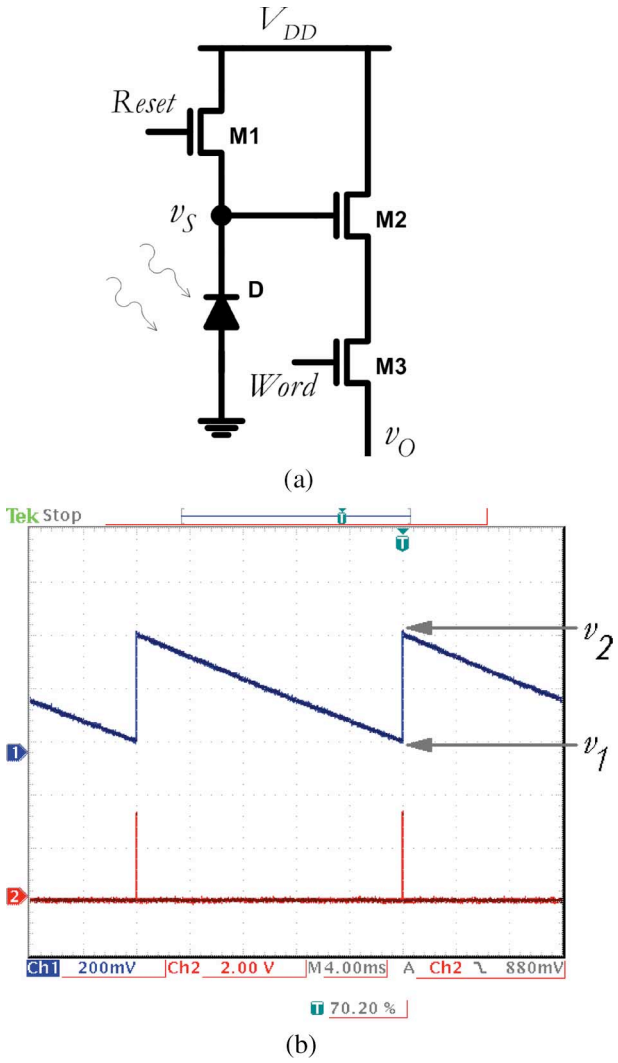


Fig. 3. (a) Structure of a three-transistor APS. (b) Reset signal, and output of the APS, captured on the oscilloscope screen. ν_1 is the output voltage at the end of integration, and ν_2 is the output voltage at the end of reset.

n+p-subjunctions, made separately for the C–V measurements, from three different dies at two frequencies. Fig. 2(a) shows the C–V curves obtained from our measurements. In order to extract m, according to (8), one can plot $\log(C)$ versus $\log(\nu+\varphi)$ and relate m to the slope of the curve. However, the actual value of φ is unknown. Multiple plots can be made for different values of φ. The curve that is closest to a straight line corresponds to the φ closest to the actual built-in potential of the junction. Fig. 2(b) suggests $m \approx 3.6$, proving that $m = 4$ can be used to describe the diode's C–V characteristic.

Fig. 3(a) shows the APS circuit. During reset, transistor M1 is turned on to bring the sense node voltage (ν_S) up close to $V_{\rm DD}$. During integration, M1 is opened (in OFF-state) and the capacitance of the photodiode D will be discharged by its internally generated photocurrent $i_{\rm PH}$ and dark current $i_{\rm DK}$. In a pinned photodiode APS, a transfer gate is used to transfer the charge to a readout node. In the three-transistor structure of Fig. 3(a), which is considered in this paper, the charge is read directly from the sense node. An equation describing the sense node voltage during integration can be written as

$$\frac{d\nu_S}{dt} = -\frac{i_{\rm PH}(t) + i_{\rm DK}(t)}{C\left(\nu_S(t)\right)}. \tag{9}$$

Assuming constant photocurrent and dark current, and (8) for the voltage-varying capacitance of the photodiode, then (9) has a closed form solution. This solution is different for different values of m. Table I shows different closed form solutions for (9), where ν_2 is the value of ν_S at the beginning of integration [Fig. 3(b)]. Note that these formulas are valid before saturation of the pixel. In the case of saturation, the diode current relation should replace the fixed $i_{\rm DK}$ in (9) to obtain ν_S.

The choice of m has a significant effect on the analytically derived sense node voltage. Fig. 4 shows different analytic solutions of Table I for ν_S, assuming different values of m. The curves deviate more as time increases. We have fabricated an APS which will be described in the next section. We have measured its output during integration, which is also shown in Fig. 4. A good agreement exists between measured output and the analytic predictions obtained by solving (9) for $m = 4$.

B. DC Level Operation of APS

At low levels of light, the APS has poor performance, which is due to its low SNR. A general SNR curve of APS versus

TABLE I
CALCULATED $\nu_S(t)$ FOR DIFFERENT VALUES OF m. NOTE THAT THE SENSE NODE VOLTAGE FOR $m = 4$ IS WHAT WAS EXPERIMENTALLY FOUND IN THE ACTUAL DIODE USED IN THIS PAPER

m	Junction	Sense node voltage (v_S)
∞	Ideal	$v_2 - \frac{i_{DK} + i_{PH}}{C_0} t$
2	Abrupt	$v_2 - \frac{i_{DK} + i_{PH}}{C_0} t + \frac{(i_{DK} + i_{PH})^2}{4C_0^2} t^2 (v_2 + \varphi)^{-1}$
3	Linear	$[(v_2 + \varphi)^{2/3} - \frac{2(i_{DK} + i_{PH})}{3C_0} (v_2 + \varphi)^{-1/3} t]^{3/2} - \varphi$
4	Actual	$[(v_2 + \varphi)^{3/4} - \frac{3(i_{DK} + i_{PH})}{4C_0} (v_2 + \varphi)^{-1/4} t]^{4/3} - \varphi$

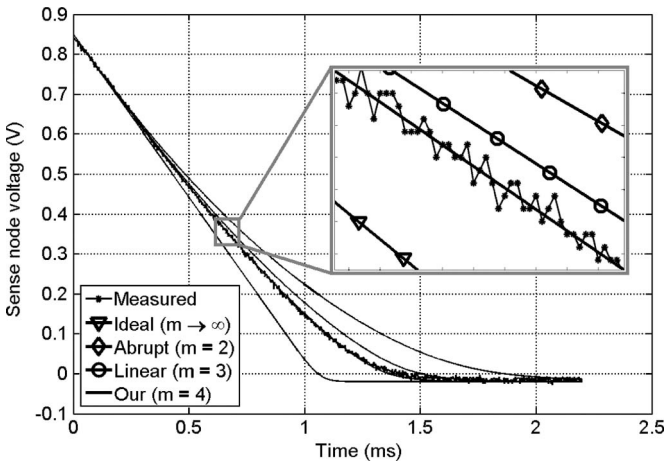


Fig. 4. Measured and calculated sense node voltage of APS (ν_S) versus time. The curves have been zoomed to better show the agreement of the measurement with the analytically calculated curve, obtained with $m = 4$ in the C–V model of the photodiode junction capacitance. The other three curves with $m = 2$, 3 and ∞ show significant deviation from the measured ν_S versus time characteristics.

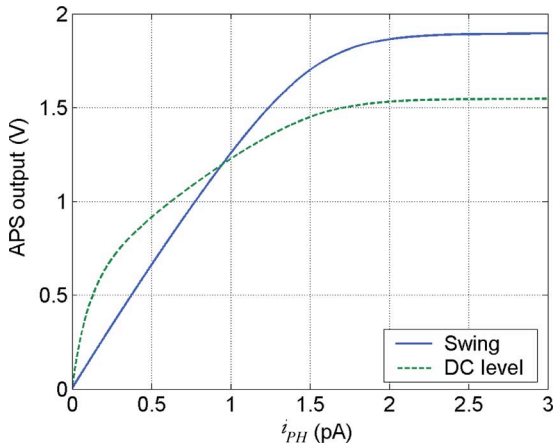


Fig. 5. Swing of the output of the APS ($\nu_2 - \nu_1$) compared to the dc level $(\nu_2 + \nu_1)/2$. For $i_{\rm PH}$ of hundredths of pA, the dc level is more sensitive. However, it saturates faster at higher levels of light, and provides lower overall dynamic range. The curves show the displacement of the signal from dark level [15].

photocurrent has been reported in [27]. It suggests an SNR of 6 dB for light powers of about 1 μW/cm^2. At 0.1 μW/cm^2, the SNR is close to 0 dB. This is the lower bound of detectable light power that is usually observed for APS of a conventional size and integration time.

The sensitivity of the pixel can be improved by increasing the size of the pixel, or lengthening the integration time. This however, may not be practical in applications that require high spatial resolution, or fast response of the photodetector.

The voltage drop during integration of APS is considered its output. This is the swing of signal, $(\nu_2 - \nu_1)$, in Fig. 3(b). In [15], we proposed that the dc level of the sense node, $(\nu_2 + \nu_1)/2$, can be considered the output of the APS. This dc level is analytically obtained by solving the reset equation of the sense node, which calculates ν_2 given ν_1 and the reset time, together with the equation of Table I, which calculates ν_1 given ν_2 and the integration time (see the Appendix). The analytically obtained dc level and swing signals versus photocurrent are shown in Fig. 5.

During the short reset time, the reset transistor is not able to completely charge the photodiode's capacitance. This means that the sense node voltage will not reach the ideal value of $V_{\rm DD}$ at the end of reset. In the conventional operation of APS, this is an unwanted phenomenon called image lag. Due to image lag, the sense node voltage is dependent on the levels of light read by the detector at the previous frames, as the reset transistor is not fully resetting the sense node voltage to $V_{\rm DD}$. Correlated double sampling (CDS) is used to take an extra sample of the sense node voltage, which is ν_2 in Fig. 3(b), to remove image lag. In our proposed method however, this phenomenon is used to our advantage, as it causes the dc level of the sense node voltage to be dependent on the power of incident light. For an APS illuminated with low levels of light, which is the focus of this paper, analysis and experiment show that the dc level of the sense node voltage can have a significant displacement from $V_{\rm DD}$, while the swing stays very close to zero. This dc level displacement is shown in Fig. 5, which demonstrates that the change of the dc level output is sharper (higher slope) than the swing at low photocurrents. However, the dynamic range of its output is smaller. To overcome the reduced dynamic range,

one option is to have a dual mode pixel that switches from the dc level mode to the swing mode at higher levels of light.

The dc level mode of operation uses the lag of the normal APS swing mode to its advantage. However, this does not mean that the dc level output is itself free of lag. Every time that the level of incident light changes, it takes a few integration and reset cycles for the dc level to converge to the new value. Based on our experimental observations, at most six integration and reset cycles are required for this convergence. This worst case happens when the light changes from total darkness to the maximum detectable level. However, for typical light-level variations, it takes about two to three cycles for the dc level to reach the stable value. Compared to the normal APS mode with CDS, which produces the correct output at the end of each integration cycle, the dc level mode of operation is slower with respect to temporal changes in the incident light.

In order to verify the performance of the dc level output in low-light levels, its SNR should be considered. Fig. 7 shows the analytically obtained SNR curves. The noise in the swing output is the integration noise, which is dominantly shot noise. The voltage shot noise power during integration is given by

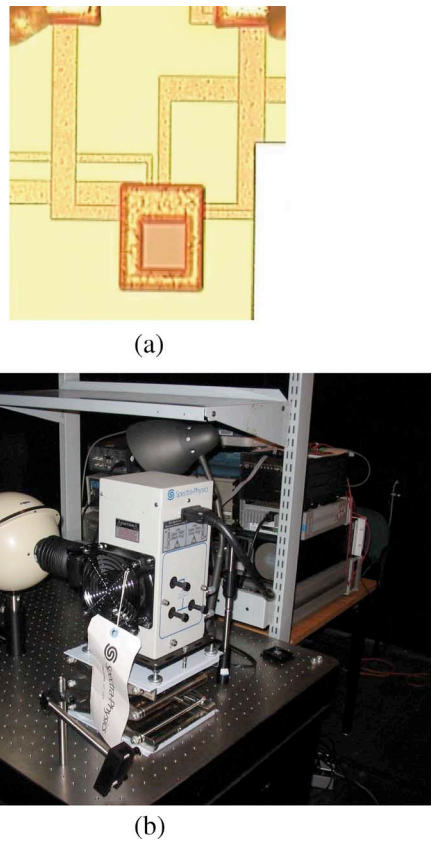
$$\overline{V_n^2} = \frac{q(i_{\rm PH}+i_{\rm DK})}{C_0^2} t_{\rm int}\left(1-\frac{1}{4(\nu_0+\varphi)}\frac{i_{\rm PH}+i_{\rm DK}}{C_0}t_{\rm int}\right) \quad (10)$$

where $t_{\rm int}$ is the duration of the integration cycle [15]. The reset noise is dominantly thermal noise and is given by

$$\overline{V_n^2} = \frac{kT}{2C_0} \quad (11)$$

where k is the Boltzmann's constant and T is the temperature [30]. The CDS removes the reset noise from the swing output. However, integration noise and reset noise will both contribute to the noise of the dc level. During each integration or reset stage, the noise adds up to the residual noise that already existed in the ν_S generated in the previous stages. These noise sources form an autoregressive noise power in the dc level. A more detailed derivation of the noise of the dc level can be found in the Appendix.

Before proceeding to the results of our design, it is useful to make a distinction between modern high-resolution APS designs, and the low-light-level detection APS designs. Modern APS designs, which mainly target imaging and photography applications, have achieved Mega-pixel resolutions. Noise floors as low as 42 [25], 29, 13, and 5 eRMS [26] have been reported for such designs. We have measured a noise floor of 106 eRMS for our APS with a 400 μm^2 photodiode size at 30 ms integration time, operating in dc level mode. The noise floor of an APS pixel has two components—a reset part and an integration part. The reset part is eliminated by CDS, and the integration part decreases as the size of the pixel is reduced. This is one of the reasons for the low noise floors reported in the above pixels, which have photodiode sizes in the range of 10 μm^2. In the dc level approach, CDS is not applied, and the total noise power has both reset and integration components, as described in the Appendix and given in (18). This is why the noise floor of our approach may be higher. However, a low noise floor does not guarantee low-light-level sensitivity. Rather, it is the ratio of the signal generated by the pixel to its noise that determines its sensitivity of the detection circuit. Our pixel using the dc level approach, has better SNR compared to the swing voltage, and thus better sensitivity to low levels of light, despite its higher noise floor. For example, it can be seen in Fig. 5 that for the photocurrents in the range of 0.1 pA and lower, the signal that can be generated using the swing approach is negligible. Also, as the level of light becomes very small, the signal generated using the dc level can be more than 20 times higher than the swing, thus providing a higher SNR and better light sensitivity.



(a) (b)

Fig. 6. We have implemented a chip in standard CMOS 0.18 μm technology. (a) Photomicrograph of our APS on the chip. (b) Optical setup in our dark room for measuring the sensitivity of the APS.

III. Experimental Results

A chip has been designed and fabricated in a commercial CMOS 0.18 μm technology for testing the APS circuit. The chip has been fabricated and packaged through Canadian Microelectronics Corporation. Fig. 6(a) shows a photomicrograph of an APS circuit on the chip. It corresponds to a pixel with a 20 μm $\times$ 20 μm photodiode size. The APS transistors are shielded with a top thick metal layer available in the standard process. The six metal connections to the APS can also be seen in Fig. 6(a). They correspond to $V_{\rm DD}$, GND, Reset, Word, and ν_O in Fig. 3(a). There is also a separate connection for the $V_{\rm DD}$ of the reset transistor, to facilitate studying the dynamic range of the pixel, and characteristics of the reset.

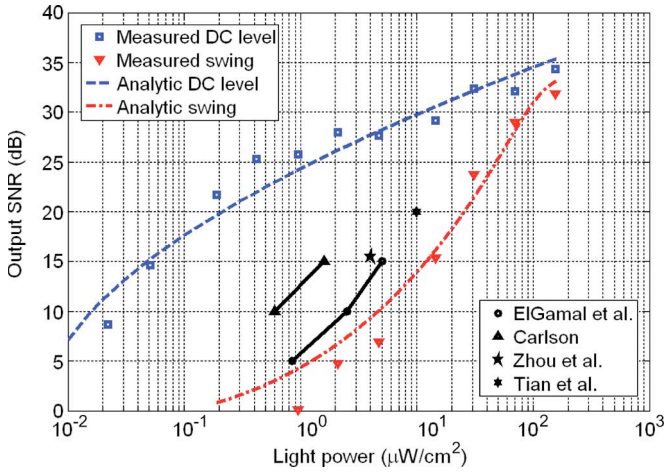


Fig. 7. Analytically-derived SNR of the APS [15], measured SNR values for our APS, and SNR values reported for some other low-light-level APS circuits in the literature. The data has been gathered from a variety of pixel sizes. The size of the pixels used in the experiments affects the reported SNR values at different light powers. The data have been adjusted to compensate for the size differences and to make a fair comparison of the different reported SNR values.

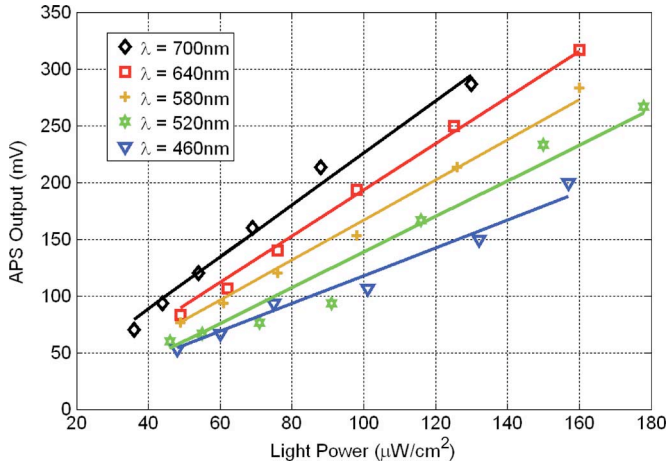


Fig. 8. Measured swing of the sense node voltage of the APS versus the power of light at different wavelengths. The curves show that the generated photocurrent of the APS approximately doubles by changing the wavelength of light in the visible range.

Fig. 6(b) shows the setup for measurements on the APS. A 75-W, Xenon lamp has been used to illuminate the APS. Xenon lamps have uniform irradiance over a wide spectrum range covering ultraviolet, visible, and near infrared. They also have good stability in the output power. The lamp is connected to the input port of an integrating sphere through a filter box. The chip is placed on a rail in front of an output port of the sphere. The optical power incident on the chip can be varied by moving it with respect to the sphere. An integrating sphere scatters light uniformly through multiple reflections along its interior, and provides nearly uniform light flux at its output.

Many precautions are needed for noise measurements. For our measurements, the optical setup was placed on a vibration-isolation table, and the fan that cools the lamp was turned off. Also, measurements were performed in an optically dark room to minimize the background illumination. The dark room in our laboratory also provides 120 dB RF shielding to minimize the external RF disturbances. Finally, stable lamp and voltage sources were used, and connections to the chip were made by triaxial cables.

Fig. 7 shows the measured SNR of the pixel. The SNR values have been evaluated by multiple measurements of the signal at each level of light. About 50–100 voltage samples are collected at each illumination level; their mean is interpreted as the signal value and their standard deviation as the noise. SNR has been evaluated for both swing $(\nu_2 - \nu_1)$ and dc level $(\nu_2 + \nu_1)/2$. The chip is illuminated at 640 nm using a narrowband filter. The light power is measured with a Newport calibrated power meter at the same wavelength. Our low levels of light power are achieved by using several attenuators in the optical path. At light powers less than 0.1 μW/cm^2, the measured power by the power meter is very noisy compared to the dc level of our pixel, which is still very stable. At these low levels of light, the output of the power meter has been sampled multiple times, and then averaged to provide the light power values shown.

Measurements in Fig. 7 show that, compared to the swing of the same pixel, the dc level of the output can detect light levels that have a power two orders of magnitude lower. The dc level has about 20 dB better SNR than the swing at about 1 μW/cm^2. The dc level output has also been compared to some SNR values of other APS circuits reported in literature. Fig. 7 shows some SNR points achieved in the work of El Gamal and Eltoukhy [27], Carlson [28], Zhou *et al.* [29], and Tian *et al.* [30]. It should be noted that parameters like the pixel size, integration time or readout rate, or the illumination spectrum affect the SNR of the APS, and they should be considered to make a fair comparison of the performance of the pixels.

Fig. 8 shows the measured variation of the output of our APS within the visible range spectrum. It shows a factor of two differences between the responses at the lower end and the higher end of the spectrum, which corresponds to doubling of the photocurrent of the APS. The power of the shot noise will also be doubled, causing an approximately 1.5 dB increase in the SNR value. Doubling the pixel area or the integration time of APS will also increase its SNR by about 1.5 dB. Appropriate changes have been made to the SNR points in Fig. 7 to account for these differences. For example, the integration times of the pixels were 30 ms in all works except in [28], which was 8 ms, for which a 3 dB correction was made to the SNR value. For the light power at the low levels of Fig. 7, the SNR of the dc level stands well above the conventional APS.

The dc level mode of operation of the APS eliminates the need for CDS. We have observed that at low light levels, the swing of the output of APS is negligible, and the output voltage looks like a dc line, as shown in [15, Fig. 2]. Thus, a single sample of the output, preferably at the middle of the integration period, is enough. Displacement of the dc level value from its dark level corresponds to the output of the pixel. It should be noted however, that if the APS has to be used in an application where temperature variation is significant over short periods of time, then the dark value of the dc level can be affected, and should also be sampled.

The dc level mode of operation of APS does not alter the pixel structure, which preserves the high fill-factor advantage of

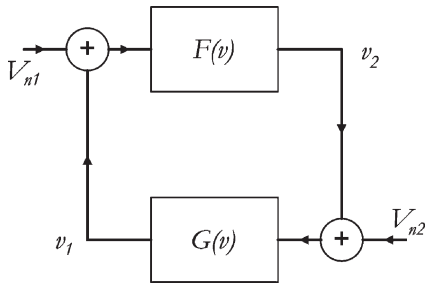


Fig. 9. Block diagram of the signal flow in the APS, showing how reset and integration noise generate the noise of the steady-state dc level.

conventional APS. The dc level performance can be improved by altering the reset mechanism. This can be achieved by decreasing the W/L of the reset transistor, decreasing the voltage applied to its gate during reset, or shortening the reset time. These changes will reduce the quality of reset, and increase the sensitivity of the dc level. Our experiments show that variation of the $V_{\rm DD}$ of the reset transistor has negligible effect on the output dc performance. Thus, the reset transistor and the source follower can share the same $V_{\rm DD}$ line. This improved sensitivity can complement the other attractive features of the CMOS photodetectors compared to PMTs, APDs, and CCDs, and can potentially replace them in many emerging biomedical applications where low-light-level sensitivity is a requirement.

IV. Conclusion

A new model for the capacitance of the photodiode in an APS was proposed. This model can produce more accurate analytical results. The model was verified by measurements on an APS fabricated in 0.18 μm standard CMOS technology. Also, measurements and calculations on our fabricated APS suggest that it can be operated in a different mode (dc level output) to get better low-light-level sensitivity. The dc level mode can detect light powers that are 30 times less than the lowest reported detectable levels using the normal APS structure. However, the dc level mode of operation responds slower to the temporal change of the incident light power. Also, the dc level mode preserves the simple APS structure and it does not need CDS. Finally, the reset time and reset transistor sizes can be adjusted to optimize the dc level sensitivity.

Appendix

The noise in the dc level output is analyzed here. The signal flow in the pixel is modeled with a periodic reset and integration system as shown in Fig. 9. $F(\nu)$ is the value of the sense node voltage at the end of reset, if the value of ν_S just before reset is equal to ν. It can be obtained by reset time analysis of the APS circuit [15] to be

$$F(\nu) = -\nu_T \ln B + \nu_T \ln\left(A\left(1 - e^{-\frac{t_r B}{\nu_T}}\right) + Be^{-\frac{t_r B}{\nu_T}} e^{\frac{\nu}{\nu_T}}\right) \tag{12}$$

where A and B are defined as

$$A = \frac{W}{LC_0} I_0 e^{\nu_G \kappa/\nu_T} \tag{13}$$

and

$$B = Ae^{-\nu_D/\nu_T} + \frac{i_{\rm PH} + i_{\rm DK}}{C_0}. \tag{14}$$

$G(\nu)$ represents the integration, and its function is given in Table I as

$$G(\nu) = \left((\nu+\varphi)^{3/4} - \frac{3(i_{\rm DK}+i_{\rm PH})}{4C_0}(\nu+\varphi)^{-1/4} t_{\rm int}\right)^{4/3} - \varphi. \tag{15}$$

Solving the feedback loop of Fig. 9, for fixed values of photocurrent, dark current, integration time, and reset times, will result in the steady-state values of ν_1 and ν_2 and dc level.

V_{n1} and V_{n2} of Fig. 9 are the integration and reset noise sources, respectively, which are added to the sense node voltage at each stage. The noise in the dc level will be obtained by calculating the contribution of these noise sources to $(\nu_2 + \nu_1)/2$. For noise calculations, each block in Fig. 9 can be replaced by its small signal equivalent

$$F(\nu + V_n) = F(\nu) + \left.\frac{\partial F}{\partial \nu}\right|_{\nu} V_n = F(\nu) + \alpha V_n \tag{16}$$

and

$$G(\nu + V_n) = G(\nu) + \left.\frac{\partial G}{\partial \nu}\right|_{\nu} V_n = G(\nu) + \beta V_n. \tag{17}$$

The feedback loop can be solved for the input sources of V_{n1} and V_{n2}, and the output defined as $(\nu_2 + \nu_1)/2$ to get

$$\overline{V_n^2} = \frac{1}{4}\left(\overline{V_{n1}^2}\,\frac{\alpha^2\beta^2 + \alpha^2}{1 - \alpha^2\beta^2} + \overline{V_{n2}^2}\,\frac{\alpha^2\beta^2 + \beta^2}{1 - \alpha^2\beta^2}\right) \tag{18}$$

where α and β are the differentials of F and G at their bias points as defined in (16) and (17). Equation (18) shows how the power of the noise in dc level is calculated with the power of integration and reset noise of APS known.

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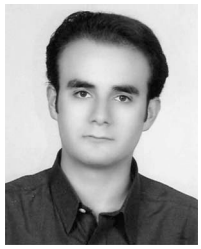


Naser Faramarzpour (S'06) was born in 1980. He received the B.Sc. degree in electrical engineering from Sharif University of Technology, Tehran, Iran, in 2002, and the M.Sc. degree in electrical engineering from McMaster University, Hamilton, ON, Canada, in 2004, where he is currently working toward the Ph.D. degree.

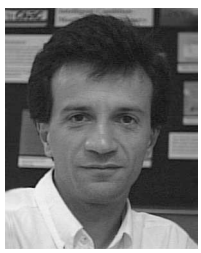
His research interests include ultrasensitive photodetector design and device modeling.

Mr. Faramarzpour was a recipient of a silver medal in the 10th International Olympiad in Informatics held in Setubal, Portugal, in August 1998, an outstanding thesis award for his master's thesis in March 2004, the Nortel networks scholarship in May 2006, and the Ontario graduate scholarship in May 2007.

M. Jamal Deen (S'81–M'86–SM'92–F'03) was born in Guyana, South America. He received the Ph.D. degree in electrical engineering and applied physics from Case Western Reserve University, Cleveland, OH, in 1985. His Ph.D. dissertation was on the design and modeling of a new coherent anti-stokes Raman scattering spectrometer for dynamic temperature measurements and combustion optimization in rocket and jet engines, and was sponsored and used by NASA, Cleveland.

He is currently a Professor of Electrical and Computer Engineering, McMaster University, Hamilton, ON, Canada, and holder of the Senior Canada Research Chair in Information Technology. His research record includes about 370 peer-reviewed articles (about 80 are invited), 14 invited book chapters and six awarded patents. His research interests are microelectronics/nanoelectronics and optoelectronics and their emerging applications.

Dr. Deen is the elected Director of the Micro- and Nano-Systems Laboratory at McMaster University. He was a Fulbright Scholar (under the Latin American scholarship program) from 1980 to 1982, an American Vacuum Society Scholar from 1983 to 1984, and a Natural Sciences and Engineering Research Council Senior Industrial Fellow in 1993. He was awarded the 2002 T.D. Callinan Award from the Electrochemical Society; a Humboldt Research Award from the Alexander von Humboldt Foundation in 2006; an IBM Faculty Award in 2006; and has won six best paper awards. He is a Distinguished Lecturer of the IEEE Electron Device Society. He is currently an Editor of IEEE TRANSACTIONS ON ELECTRON DEVICES; Executive Editor of *Fluctuations and Noise Letters*; and Member of the Editorial Boards of The *Journal of Nanoelectronics and Optoelectronics*, the *Microelectronics Journal, Open Journal of Applied Physics* and the *International Journal of High Speed Electronics and Systems*. He has been elected a Fellow of the Royal Society of Canada; a Fellow of the Canadian Academy of Engineering, a Fellow of the Institute of Electrical and Electronic Engineers; a Fellow of the Electrochemical Society; a Fellow of the American Association for the Advancement of Science; a Fellow of the Engineering Institute of Canada; and Honorary Member of World Innovation Foundation—the Foundation's highest honor.



Shahram Shirani (S'88–M'89–SM'04) received the B.Sc. degree in electrical engineering from Esfahan University of Technology, Isfahan, Iran, in 1989, the M.Sc. degree in biomedical engineering from Amirkabir University of Technology, Tehran, Iran, in 1994, and the Ph.D. degree in electrical and computer engineering from the University of British Columbia, Vancouver, BC, Canada, in 2000.

Since July 2000, he has been with the Department of Electrical and Computer Engineering, McMaster University, Hamilton, ON, Canada, where he is an Associate Professor. His research interests include image and video compression, imaging systems, multimedia communications, and ultrasonic imaging.

Dr. Shirani is a Registered Professional Engineer (P.Eng.).

Qiyin Fang (M'06) received the B.S. degree in physics from Nankai University, Tianjin, China, and the M.S. degree in applied physics and the Ph.D. degree in biomedical physics from East Carolina University, Greenville, NC.

Prior to joining McMaster, he was a Research Scientist in the Department of Surgery, Cedars-Sinai Medical Center, Los Angeles, CA. He is currently an Assistant Professor of Engineering Physics at McMaster University, Hamilton, ON, Canada, and holds a junior Canada Research Chair in Biophotonics. His current research interests are in the general field of biophotonics including optical spectroscopy and imaging guided minimally invasive diagnostic and therapeutic devices, miniaturized MOEMS sensors and imaging systems, and advanced optical microscopy and their emerging applications.

Louis W. C. Liu was born in Hong Kong and came to Canada in 1984. He received the Bachelor's and the Master's degrees in engineering physics from McMaster University, Hamilton, ON, Canada. His thesis, titled *Pacemaker Activity and Intercellular Communication in the Intestinal Muscular*, earned him a Ph.D. degree, in 1995.

He remained at McMaster University where he completed his medical training and received the Doctor of Medicine in 1998. He completed his Internal Medicine Residency Training at the University of Toronto and his Gastroenterology subspecialty fellowship training at McMaster University. He is currently an Assistant Professor in the Department of Medicine at the University of Toronto. He has published 17 peer-reviewed articles and three book chapters.

Dr. Liu was awarded with the Clinician Scientist Award from the Canadian Institute of Health Research (CIHR) for the period between 2003 and 2007. He has received ten research awards; four of which were selected from international Scientific Meetings. He is currently receiving research funding from the CIHR and the Canadian Association of Gastroenterology. He has been a Fellow of the Royal College of Physicians of Canada since 2002 and licensed by the College of Physicians and Surgeons of Ontario and is currently a member of the American College of Gastroenterology, American Motility Society, Canadian Association of Gastroenterology, Canadian Association for the Study of the Liver, Canadian Medical Association and the Ontario Association of Gastroenterology.

Fernando de Souza Campos was born in Presidente Prudente, Brazil, on September 27, 1971. He received the B.E. degree in electrical engineering from Paulista Foundation of Technology and Education, in 1993. He received the M.E. degree from Federal University of Santa Catarina, Santa Catarina, Brazil, in 1995. He is currently working toward the Ph.D. degree at State University of Campinas, Campinas, Brazil.

Since 2004, he is Assistant Professor at the University of the State of São Paulo, Bauru, Brazil. His research interests are new readout circuits and sensors for high dynamic range imaging applications.

Jacobus W. Swart (S'76–M'77–SM'90) received the B.Engineer and Dr.Engineer degrees from the Polytechnic School of the University of São Paulo, Brazil, in 1975 and 1981, respectively.

After his Dr.Engineer degree, he worked at the following institutions: K. U. Leuven, Belgium, 1982–1983, as a Postdoctoral Fellow; CTI, Campinas, 1984, as Head of Process Engineering; LSI-University of São Paulo, 1985–1988, as Assistant Professor; SID Microeletrônica, 1986, as part-time Researcher; RTI, USA, 1991, as a Visiting Scientist and State University of Campinas, since 1988, currently, as a Full Professor. He served as Director of the Center for Semiconductor Components, from April 1998 to April 2005. Recently, he has been appointed as Director of CenPRA, an IT research center in Campinas. He worked on charge-coupled device, nMOS, CMOS, and HBT process integration, device characterization and modeling, gettering processes, plasma processes, rapid thermal processes, silicide formation and characterization. His current research activities and interests include CMOS, HBT, and MEMS devices, process integration, and process modules such as plasma processing, thin gate dielectrics and rapid thermal anneal processes. He has published over 40 papers in International Journals and 35 full papers in Proceedings of International Conferences, about 100 full papers in Proceedings of Regional Conferences, besides over 70 abstracts at conference proceedings. He has presented about 50 invited and/or tutorial lectures at different conferences, workshops and visits. He has advised 30 Dr. and M.Sc. degree students. He is ranked as Fellow Researcher, level 1A (highest), at Conselho Nacional de Desenvolvimento Científico e Tecnológico.

Dr. Swart is a member of ECS, SBMicro, and SBMO and has been President of SBMicro twice, 1988–1990 and 1998–2000. He is currently the Head of a large research network in Brazil, called NAMITEC.