A Novel, High-Dynamic-Range, High-Speed, and High-Sensitivity CMOS Imager Using Time-Domain Single-Photon Counting and Avalanche Photodiodes

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***Abstract*—Avalanche photodiodes used in Geiger mode as single-photon counters have become very attractive imaging tools. High-speed single-photon imaging can be used in very low-light-level applications such as surveillance and security imaging, quantum computing, and biomedical imaging including bioluminescence and fluorescence lifetime imaging. However, a typical avalanche-based single-photon detector cannot offer the high dynamic range that is needed for many biomedical and surveillance applications. In this paper, we show how a single-photon detector can be used in time domain for high-dynamic-range applications. We also discuss novel techniques to implement the time-domain single-photon imager in mainstream deep-submicrometer CMOS technology. The designed imager offers high dynamic range and high sensitivity, while maintaining high-speed operation and low cost.**

***Index Terms*—Avalanche photodiodes (APDs), CMOS image sensor, integrated photodetector, silicon avalanche photodiode (SAPD), silicon photodetector, single-photon detectors, single-photon avalanche detectors (SPADs), time-domain (TD) image sensor.**

I. Introduction

TIME-DOMAIN (TD) imaging using an active-pixel sensor (APS) is a technique that can be used to enhance the dynamic range of a detector [1], [2]. In TD imaging, the output voltage of the APS is compared with a reference voltage and the time required for the APS to drop below that reference voltage is recorded. A strong optical signal will have a shorter acquisition time than a weak one, and the dynamic range is the ratio of maximum acquisition time to the minimum time.

One of the main drawbacks of TD imagers is the tradeoff between frame rate and dynamic range. Fig. 1(a) shows an example of the output of an APS for four different optical powers, corresponding to photocurrents of 1 nA, 1 pA, 100 fA, and 10 fA, which give a dynamic range of 100 dB. The calculations in the figure assume a zero or negligibly small dark current value. Neglecting the noise sources, the following relationship describes the waveform of the photodiode voltage v_d of a typical APS:

$$v_d(t) = V_{\mathrm{DD}} - \left(\frac{i_{\mathrm{ph}} + i_{\mathrm{dark}}}{C_d}\right) t \tag{1}$$

where V_{DD} is the supply voltage, i_{ph} is the generated photocurrent, i_{dark} is the dark current of the photodiode, t is the pixel integration time, and C_d is the capacitance of the photodiode. Assuming a V_{DD} of 1.8 V and a C_d of 150 fF, the pixel conversion rate $(1/t)$, with a constant reference voltage of half the supply voltage, would depend on the integration time t required for the weakest light signal, giving a rate that is $1/t = 1/13.5\ \mathrm{s} = 0.074$ conversions/s for a dynamic range of 100 dB. If a variable reference voltage is used, such as a ramp threshold voltage, for weaker signals, the pixel conversion rate can almost be doubled, as shown in Fig. 1(a). However, even with the doubled pixel rate, this technique is inadequate for high-speed applications.

In this study, we describe the design of a novel imager that uses time-domain single-photon counting (TDSPC).[1] Fig. 1(b) shows the electron count equivalent of Fig. 1(a), which can be calculated using

$$n(t) = \left(\frac{i_{\mathrm{ph}} + i_{\mathrm{dark}}}{e}\right) t \tag{2}$$

where n is the electron count during the integration time t, and e is the electron charge. Such electron counts can be generated using single-photon-counting Geiger-mode avalanche photodiodes (APDs). When using a constant count threshold of 512, the pixel conversion rate is 1/8 ms $= 125$ conversions/s for the same dynamic range of 100 dB. This shows a speed improvement of three to four orders of magnitude for both the constant and variable threshold methods. For the 1 pA photocurrent shown in Fig. 1(b), a time of 82 μs is required to reach a threshold count of 512 (dashed line in Fig. 1(b)). This can be converted back to Fig. 1(a) by evaluating (1) for a current of 1 pA and an integration time of 82 μs. In this case, the APS voltage drop can be calculated from (1) as 547 μV, which is below the detection limit of a simple in-pixel circuit. On the other hand, counting 512 events in a single-photon counter, which counts pulses in digital format, is quite straightforward [3]–[11]. This shows how the novel TD single-photon imaging (TDSPI)

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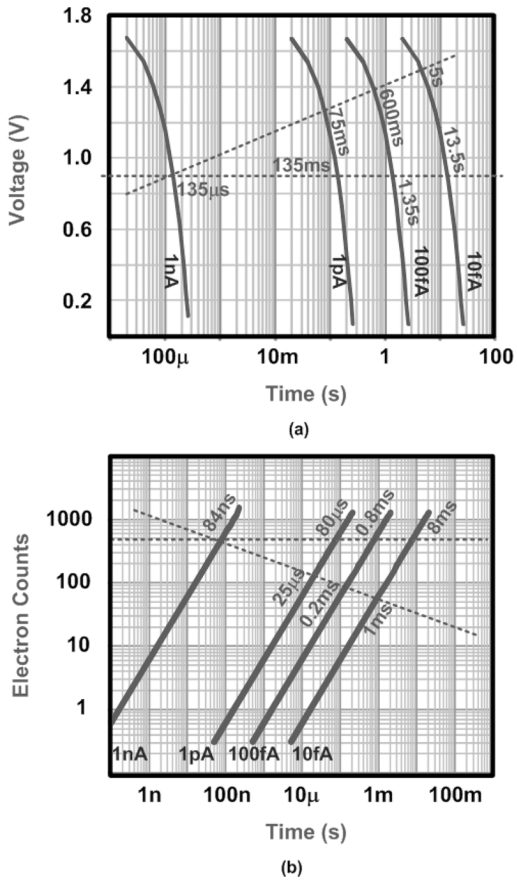

Fig. 1. (a) Calculated APS output voltage for four different optical signals showing the generated photocurrents and the corresponding times required to drop below the threshold voltage. (b) Electron count equivalent of (a).

technique can achieve high dynamic range while maintaining a reasonable frame rate that is at least three orders of magnitude higher than the conventional high-dynamic-range imaging techniques.

It is noted, however, that in both conventional APS [12], [13] and single-photon counting time-domain imagers, the weak signals are limited by the dark current and dark count. The dynamic range of the imager will have the upper bound limited by the single photon avalanche detector's (SPAD's) deadtime and lower bound limited by its dark count. In order to maintain a reasonable signal-to-noise ratio, the weakest detectable signal should typically have a photon count that is around ten times the dark count. Based on the weakest signal used in Fig. 1, the maximum dark count should be below 6 kHz, which is reasonable for CMOS SPADs [4], [6]–[10].

Using the combination of SPC Geiger-mode APDs and a novel TD counting technique, we have designed CMOS-based imagers that are of high speed, high sensitivity, and wide dynamic range. Details of our design are presented in the following sections. In Section II, the proposed TDSPC pixel design is described, while in Section III the design of an analog counter for in-pixel counting that allows for parallel pixel processing while maintaining a reasonable fill-factor (FF) is discussed. The pixel and imager layouts are shown in Section IV, and, finally, the conclusions are presented in Section V.

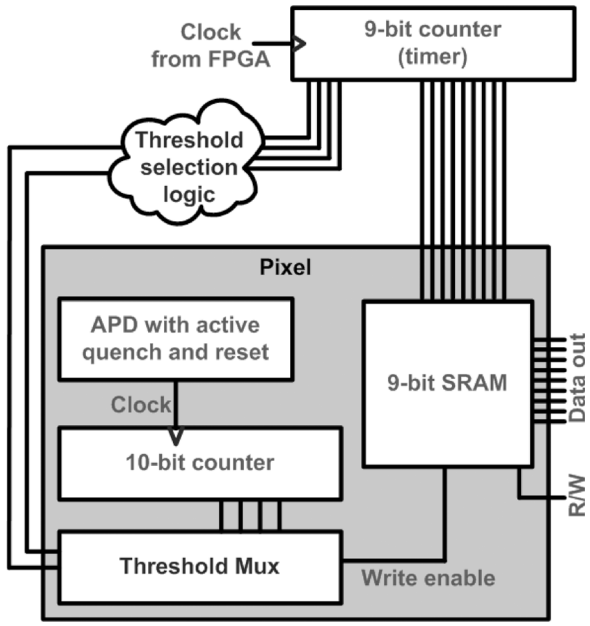

Fig. 2. Block diagram of the TDSPC pixel.

II. TDSPC Pixel Design

The TDSPC pixel conversion rate is related to the frame rate based on the number of pixels in the array and the readout time. A very basic implementation of the TDSPI would be to use an array of single-photon detectors that are connected through multiplexing to one common counter for the entire array. In this case, rather than counting for a fixed integration time, the counting will continue until a selected threshold is reached. Using this technique however, based on the calculations shown in Fig. 1, for a 100-dB dynamic range and a 125-conversions/s pixel conversion rate, would mean that eight seconds are needed for the conversion of an array of 1000 pixels, which is a very long time for such a small array. Therefore, in order to maintain a high frame rate, simultaneous in-pixel counting and threshold detection are needed.

Fig. 2 shows a block diagram of the TDSPC pixel that allows for simultaneous pixel counting and conversion in each pixel and, thus, for high-speed operation [3]. Each pixel contains a low deadtime Geiger-mode active quench and reset single-photon avalanche detector (SPAD) [5], an in-pixel counter with threshold detection, a threshold selection multiplexer, and a static random access memory (SRAM). The output of the global timer, which is connected to all pixels, is sampled and stored in the pixel SRAM once the threshold count in the pixel is reached. The timer is clocked at a fixed rate from an external clock provided by a field-programmable gate array (FPGA) that interfaces to the imager for control and data processing.

As the count of the global timer increases, the threshold selection logic reduces the count threshold for in-pixel counting by controlling the threshold multiplexer. Initially, the threshold multiplexer monitors the most significant bit of the counter and as the count threshold is reduced, the multiplexer moves from the most significant bit to the bit before, and so on. The block diagram is simplified, and details such as logic circuit elements

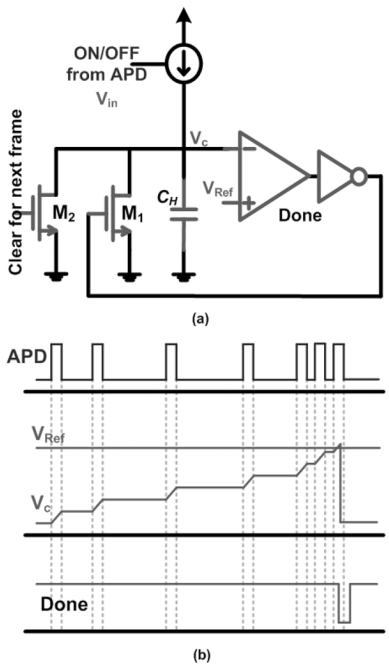

Fig. 3. (a) Schematic diagram of the designed analog counter. (b) Waveform of the operation of the analog counter.

that control the counter and stop the count once the threshold is reached, are omitted. Finally, a frame is completed once the maximum time is reached or once all pixels have completed the threshold detection, which can be checked by the occurrences of the write-enable signals from all pixels in the array. After the frame conversion is complete, the readout of the SRAM values uses conventional array access and is very fast, of the order of a few nanoseconds per pixel.

The pixel shown in Fig. 2 is quite complex. In this design, more than 200 transistors per pixel are required—a large transistor count mainly due to the use of in-pixel digital counters. This makes the area of the TDSPC pixel too large to implement using current mainstream silicon technologies. However, using a specialized imaging technology and packaging, such as thin-film CMOS or 3-D integrated circuit packaging could help in the TDSPC implementation. Also, with very deep-submicrometer CMOS technology, the TDSPC pixel can be implemented with a reasonable FF. Since the in-pixel digital counter and the digital threshold detector are the components with the most number of transistors, novel in-pixel analog counting and threshold detection techniques are proposed in this work. These new circuits are discussed in Section III.

III. In-Pixel Counter Design

Fig. 3(a) shows the proposed in-pixel counter and threshold detector. The pulses from the APD, which have a fixed width equal to the deadtime τ_{SPAD} of the active quench and reset SPAD circuit, control a switched current source that charges a capacitor (C_H). The waveform in Fig. 3(b) illustrates the operation of the analog counter. With the count (n) of pulses from the SPAD, the capacitor voltage increases according to

$$V_c(n) = \frac{nI\tau_{\mathrm{SPAD}}}{C_H} + V_0 \tag{3}$$

where V_c is the voltage across the capacitor C_H and is a function of n, I is the current of the pulse-controlled current source, τ_{SPAD} is the deadtime of the SPAD circuit, and V_0 is the initial voltage of the capacitor prior to counting. Then, V_c is compared with a reference voltage V_{Ref} that acts as the count threshold. The comparison is performed using a high-speed comparator. Once the capacitor voltage exceeds the threshold voltage, the **Done** signal goes low, clearing the capacitor voltage to V_0 and restarting the count.

Although, in theory, an analog counter can provide an infinite count based on (3), using a small voltage step size, $I\tau_{\mathrm{SPAD}}/C_H$ in (3), would require an accurate comparator that is not easy to design for high-speed operation with a small area for in-pixel implementation. To avoid this issue, the count value was limited to a range of 10–30, and two counters were cascaded to obtain a count that is the product of the counts of both stages. In this way, the accuracy is preserved by a reasonable tradeoff with only pixel area.

Fig. 4(a) shows the schematic diagram of a complete two-stage analog counter. The ideal current sources that were previously shown in Fig. 3(a) have been implemented as current mirrors. Transistors M_4, M_6, and M_3 form the first current mirror that mirrors the current between transistors M_4 and M_6 to the branch between M_3 and the capacitor with a current multiplication that is equal to the ratio of the size of transistor M_3 to the size of transistor M_4. Similarly, transistors M_8, M_{10}, and M_7 form the second current mirror. The current mirrors are switched on once the pull-down transistors (M_6, M_{10}) are on and transistors M_5 and M_9 are off. Transistors M_5 and M_9 were added to ensure complete shutdown of transistors M_3 and M_7.

The first counter counts the pulses coming from the SPAD, which have a pulsewidth τ_{SPAD} that is equal to the SPAD deadtime, resetting itself once the threshold $\mathrm{V}_{\mathrm{Ref1}}$ is reached. The second counter counts the reset pulses of the first counter until the threshold voltage $(\mathrm{V}_{\mathrm{Ref2}})$ is reached and, the write enable signal is generated to the SRAM to latch the time from the global digital timer. The pulsewidth that clocks the second counter is slightly longer than the SPAD deadtime due to the limited bandwidth of the operational amplifier (opamp) in the first analog counter. For this reason, a lower current ratio was used in the current mirror of the second counter. The count threshold of each counter can be reduced or adjusted dynamically by varying the reference voltages of the comparators. At reference voltages of 1.5 V applied to both comparators, the first counter has a count of 21, while the second counter has a count of 26, which gives a total count of 546 for the two-stage in-pixel analog counter. The capacitor C_H was designed using a MOS capacitor, since it offers a small layout size of 4 μm $\times$ 3 μm with a capacitance of around 50 fF. Also, the MOS capacitor had a thick oxide in order to reduce its leakage.

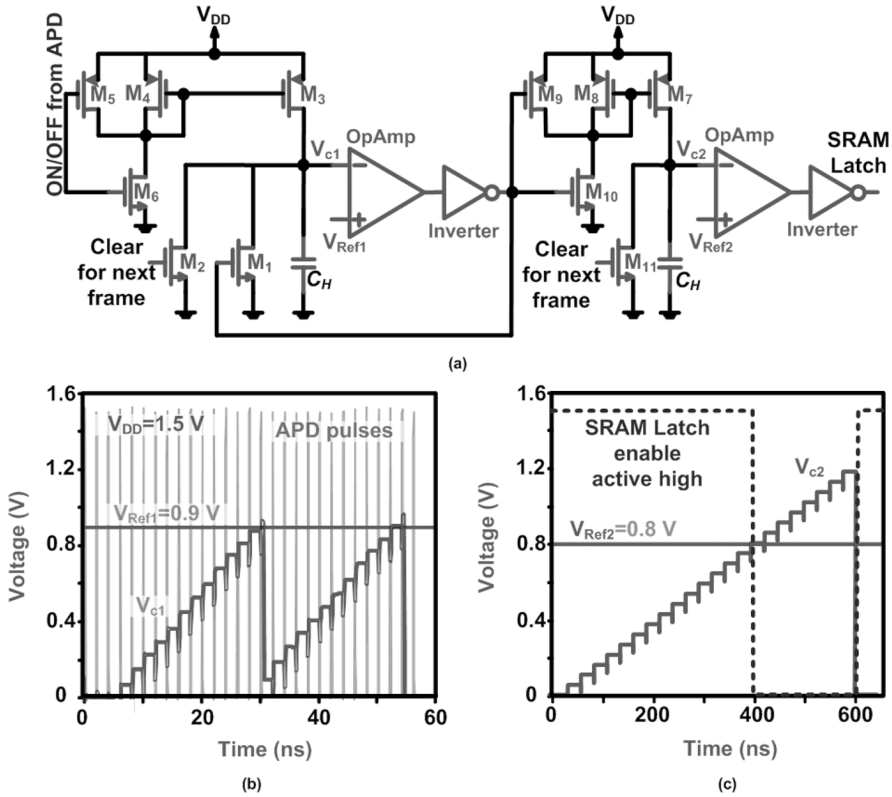

Fig. 4. (a) Two-stage analog counter schematic diagram and the simulation results of (b) the first stage and (c) the second stage showing the SRAM latch enable signal.

The SPICE simulation results of the first and second analog counters are shown in Fig. 4(b) and (c), respectively. For this circuit, SPICE models and simulations are reliable since the circuit operates at frequencies that are much lower than the cutoff frequency of the transistors used, and no major parasitic effect would be present in the chip layout. With the selected reference voltages shown in the figure ($V_{Ref1} = 0.9$ V and $V_{Ref2} = 0.8$ V), the first counter has a count of 12 and the second has a count of 15 for a total count of 180. The circuit was designed to keep the writing in the SRAM enabled until the count threshold is reached, after which the writing is disabled, thus, the counters can continue operating. In this way, the time is continuously being written to the SRAM until the threshold is reached, when the last time before the threshold will be saved. The second counter will continue to count or even saturate without consequences. Both counters are cleared at the start of the acquisition of a new frame by a global signal that turns on transistors M_2 and M_{11} for a short time in the range of 10 ns.

A high-speed small-size opamp was designed to be used as an open-loop comparator for the analog counter. Usually, in an opamp, capacitive compensation is needed to ensure that the amplifier is stable with no oscillations. Since the compensation capacitor is usually one of the largest components of the opamp, it was removed to reduce the layout area of the circuit. This was possible since the amplifier will be used as an open-loop comparator. The designed high-speed comparator consists of three stages—a differential stage, an amplifying stage, and an output stage. In order to maintain high-speed operation, the gain was obtained from three stages rather than one or two, where each stage provides a small amount of gain in order to maintain the bandwidth.

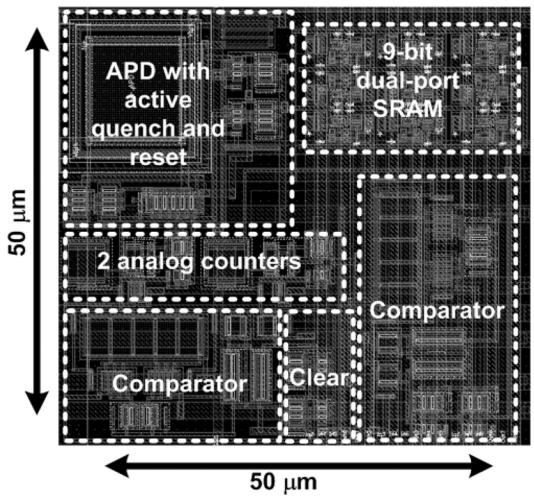

Fig. 5. Layout of a SPAD pixel with in-pixel analog counting and SRAM for parallel pixel analog-to-digital conversion.

IV. TDSPC Pixel and TDSPI Layout

Fig. 5 shows the layout of a time-domain single-photon counting (TDSPC) pixel that was implemented using a mainstream 130-nm CMOS process from IBM. The pixel occupies

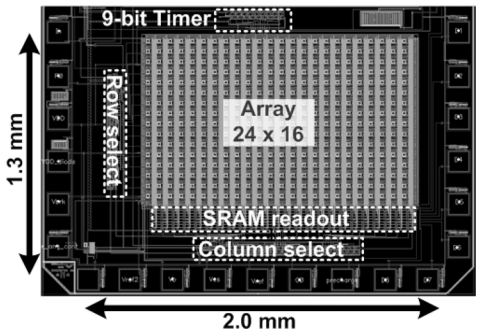

Fig. 6. Layout of the 24 × 16 pixel TDSPI with timer, readout, and array access circuits.

an area of 50 μm × 50 μm and has a FF of 4%. The pixel contains all of the components necessary for the implementation of a TDSPC imager that can achieve simultaneous counting of all pixels in parallel. The layout of the opamp measures an area that is less than 15 μm × 15 μm, and the layout of each analog counter measures an area that is less than 15 μm × 30 μm. The area occupied by this pixel design is less than most state-of-the-art SPAD designs [4]–[11], although the pixel contains counters, compared with previous designs that only contain active quench and reset circuitry. This pixel area reduction was mainly due to the compact analog counter and SPAD designs, in addition to using a deep-submicrometer technology. Potential issues with low (4%) FF can be addressed by using microlenslet arrays or fiber couplers. Initially, the SPAD alone had an FF of 25%, which was reduced to 4% in the TDSPC pixel. The effect of FF reduction can be calculated in terms of reduction in resolution. The resolution of an imager is obtained from the maximum modulation transfer function $(\mathrm{MTF}_{\max})$, which is equal to $1/(2p)$, where p is the pixel pitch. For a square pixel, the pitch and FF can be related by

$$p = \sqrt{\mathrm{AA}/\mathrm{FF}} \tag{4}$$

where AA is the active area. Finally, the imager resolution can be related to the FF by

$$\mathrm{MTF}_{\max} = \sqrt{\mathrm{FF}/4\mathrm{AA}}. \tag{5}$$

The reduction in FF causes a square-root reduction in resolution, meaning that reducing the FF of the pixel from 25% to 4%, which is a factor of 6.25, will result in a drop of 2.5 times in resolution.

The TDSPC pixel was used in a camera-on-a-chip with an array of 24×16 pixels, and it is shown in Fig. 6. The imager uses a single timer that is common to all pixels and row- and column-select circuitry, in addition to the SRAM readout circuitry. When a row is selected, the SRAM outputs of each column are placed on a 9-bit column bus that is then multiplexed by column selection onto a 9-bit row bus. The final output of the array is the contents of the 9-bit SRAM of the selected pixel.

V. Conclusion

This paper shows the design of an imager that can achieve high dynamic range and high sensitivity with frame rates that are three to four orders of magnitude higher than conventional wide-dynamic-range imagers. This was done using single-photon counting in the time domain, where the high sensitivity of single-photon counters was utilized to achieve count threshold detection. The speed was improved further using a scalable novel pixel design that can allow for simultaneous pixel counting and threshold detection. The pixel design, however, was too complicated to be implemented using the technology node (130 nm) that was used in this work while maintaining a reasonable FF. A novel in-pixel counting and threshold detection technique was implemented to reduce the complexity of the pixel using analog counters. The final pixel design had an FF of 4% and contained a 9-bit dual-port static random access memory, an active quench and reset single-photon avalanche detector, and two cascaded analog counters and threshold detectors. The pixel was laid out as a complete camera-on-a-chip TDSPI with a 384-pixel array that could achieve high dynamic range due to using TD high sensitivity due to using single-photon counting and maintain high speed due to the digital event-based counting and simultaneous pixel processing.

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