

CMOS Active-Pixel Sensor With *In-Situ* Memory for Ultrahigh-Speed Imaging

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Abstract—State-of-the-art image sensor arrays have not been able to operate at frame rates that exceed tens to hundreds of thousands of frames per second. The main bottle neck preventing imaging at higher frame rates is the time required to access the array, convert the image data from analog to digital, and transmit the data off the image sensor chip. The later is considered the most significant source of delay, mainly due to the limited number of input and output ports available on the chip. This work allows for a significant increase in image capture rate by separating the image acquisition phase from the conversion and readout phase. This was done by capturing eight frames at a high capture rate and temporarily storing the multiple frames into analog memory units that are incorporated inside the pixel. The design was implemented in a deep-submicron CMOS 130 nm technology that allows for high-speed operation. This paper discusses the tradeoffs of using *in-situ* frame storage and gives some recommendations.

Index Terms—Active-pixel-sensor, biomedical imaging, image-sensor, photodetectors, smart-pixel, ultrahigh-speed.

I. INTRODUCTION

HIGH-SPEED imaging has gained significant research interest due its wide range of applications, such as integral machine vision, time-of-flight imaging, topographic imaging, three-dimensional high-definition television (3D-HDTV), and optical molecular imaging systems, specifically fluorescence life-time imaging (FLIM) [1]. Deep submicron CMOS technology downscaling has especially made such high-speed imaging possible. One of the main advantages of CMOS image sensors is that they are fabricated in standard CMOS technologies, which allows for full integration of the image sensor along with the processing and control circuits on the same chip, leading to a reduction in power consumption, cost and overall size of the imager. Most importantly, however, CMOS downscaling has allowed for integration of new sensor functionalities, by the design of smart pixels [2]. Such smart

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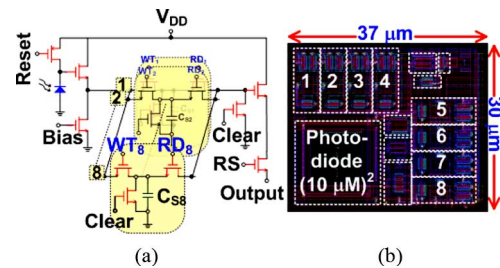


Fig. 1. (a) Schematic diagram of the ultrahigh-speed *in-situ* APS containing eight memory elements and 38 transistors and (b) layout screen capture of a single pixel with a 9% fill-factor designed using a CMOS 0.13 μm technology kit from IBM [16]. The low 9% FF is comparable to smart pixel designs such as the digital pixel sensors in [7]. The photodiode used is an n^+ / p -well with a guard ring for high-speed operation.

pixels truly utilize the potential of CMOS technology for imaging applications enabling CMOS imagers to achieve the image quality and global shuttering performance necessary to meet the demands of ultrahigh-speed applications.

Based on a comparison of some of the high-speed imagers in the literature [3]–[15], it is clear that moving to frame rates (FR) higher than 10 000 fps would require completely separating the acquisition and processing phases by relying on *in-situ* frame storage [1]. In this work, results from an ultrahigh-speed CMOS pixel that can capture eight frames using *in-situ* frame storage are presented. Full details of the pixel design are discussed, as well as the pixel measurement results with comparison to the calculated signal-to-noise ratio (SNR).

The paper is organized as follows. In Section II, the design and simulation results of the ultrahigh acquisition rate CMOS active-pixel sensor (APS) are discussed. The pixel measurement results are presented in Section III, while the calculated and measured SNRs are shown in Section IV. The scalability of the design is shown in Section V, which is followed by the conclusions in Section VI.

II. ULTRAHIGH-SPEED PIXEL DESIGN

The schematic diagram and the layout of the pixel, which contains 38 transistors, are shown in Fig. 1 [16]. The basic idea is to utilize eight analog memory units *in-situ* to temporarily hold eight frames at a very high acquisition speed, avoiding the delay time in analog-to-digital conversion and readout. The write switches (WT) that select which storage element to use also serve as global shutters. The storage elements C_{S1} to C_{S8} were implemented using MOS capacitors to reduce layout area;

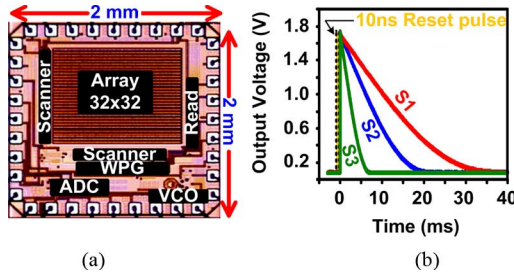


Fig. 2. (a) Photomicrograph of the ultrahigh-speed camera-on-a-chip fabricated in a 130 nm CMOS technology and (b) measured APS output voltage at different illuminations ($S_3 > S_2 > S_1$) using a 10 ns reset pulse.

they have a capacitance of 60 fF and were designed using thick-oxide (5.2 nm) transistors to reduce leakage.

In [1], we have shown simulation results of the ultrahigh-speed APS to test the electrical limit. The eight frames were acquired within roughly 7 ns, making this imaging technique suitable for fluorescence lifetime imaging. If repeated experiments were needed for low-light level measurements, the consecutive frames can be accumulated in the capacitor without clearing the previous frames. The amount of light required to generate the simulated voltage drop depends on the light sensitive device used. It is recommended to use an avalanche photodiode or a single photon detector for best sensitivity.

III. PIXEL MEASUREMENT RESULTS

A complete-camera-on-a-chip design occupying an area of $2 \text{ mm} \times 2 \text{ mm}$, shown in Fig. 2(a), was fabricated with an array of 32×32 ultrahigh-speed pixels. In addition to the row and column scanners that are needed for array access, this imager required an on-chip implementation of high-speed clocking and conversion circuitry. This circuitry includes a read sequencer, write pulse generator (WPG), high-speed ADC and on-chip voltage controlled oscillator (VCO) to generate the high-speed clocks. The VCO is a cross-coupled negative- g_m 3-GHz oscillator, which clocks the ADC and the write pulse generator circuits. The Read circuit is a shift register that is clocked externally to provide the control signals to the pixels. This was done to reduce the number of I/O pads needed.

Since the image capture rate is very high, the photodiode reset and analog memory write pulses cannot be provided externally. Rather, they are generated internally and initiated by an external start signal. The triggering is done using an edge-triggered circuit that accepts an external start signal as an input. When the start pulse occurs, the circuit generates the 8 reset pulses and the 8 write signals between the reset pulses that have a width of 400 ps each (controlled by the clock).

The implemented ADC uses a high-speed dual-slope integrating method with a ramp resistor and capacitor equal to $20 \text{ k}\Omega$ and 2 pF , respectively. The ADC is clocked by the on-chip 3 GHz VCO and uses an 8-bit counter for a maximum conversion time that requires 128 ns. The calculated frame rate is 7629 fps.

The output of the APS pixel, shown in Fig. 2(b), was measured by controlling one of the memory elements. In this case,

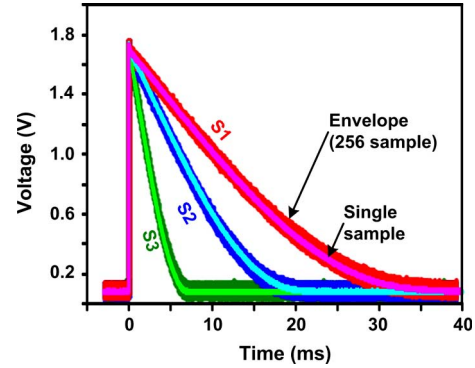


Fig. 3. Measured APS output voltage for different illuminations showing both a single sample measurement and the envelope of 256 samples.

WT_1 and RD_1 were turned on, while all other switches were turned off. An active low reset pulse was applied to the PMOS reset transistor with a pulse duration of 10 ns. The figure shows how the response changes with increasing the light intensity and the measurement shows how the pixel responds well to a high-speed reset pulse.

IV. SNR RESULTS

There are a number of noise sources in an APS pixel. A good estimate for the amount of noise available at the output of the APS is obtained by recording the output voltage for 256 measurements. In Fig. 3, these measurements are overlapped with a single sample measurement for comparison. It can also be seen that the noise increases with integration time, which is mainly due to the integration noise, as will be shown by (1). The dominant noise during the reset phase is the thermal noise from the on-resistance of the reset transistor. The thermal noise voltage ($k_b T / C_{PD}$) depends on the diode capacitance and temperature, but not on the on-resistance of the transistor. This is because although the increase in on-resistance results in an increase in thermal noise voltage, it also results in a reduction in bandwidth, which cancels out. To achieve soft reset, an NMOS reset transistor rather than a PMOS can be used to reduce the thermal noise by \sim half [14]: however, soft reset can lead to image lag from frame to frame [17]. During the integration phase, the dominant noise is shot noise due to the dark current (i_{dark}) and the photocurrent (i_{PD}). Assuming that the photodiode capacitance (C_{PD}) is constant over the integration period (t_{int}), the noise voltage at the end of the integration time is given by

$$\overline{v_n^2} = \frac{q(i_{PD} + i_{\text{dark}})t_{\text{int}}}{C_{PD}^2} \quad (1)$$

The noise sources available in this APS structure are similar to the standard 3T-APS in terms of reset noise and integration noise. However, the readout noise is different since there is a transfer from the photodiode to the storage capacitor phase, as well as a transfer from the storage capacitor to the column phase (Fig. 4).

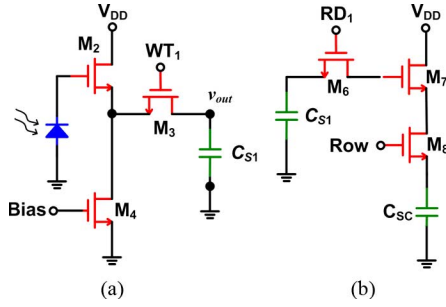


Fig. 4. (a) Photodiode to storage capacitor readout equivalent circuit and (b) storage capacitor to column readout equivalent circuit.

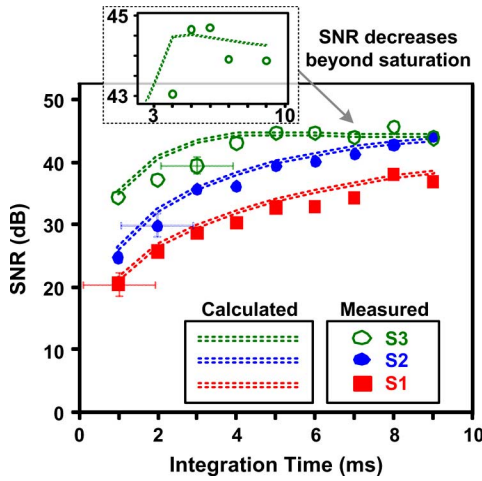


Fig. 5. Measured and calculated SNR for three different illuminations. The inset figure shows a close up to S3 illustrating that the SNR drops beyond saturation.

The readout noise for Figs. 4(a) and 4(b) can be calculated based on the following two equations, respectively, assuming constant C_{S1} and C_{SC} capacitors:

$$\begin{aligned} \overline{V_{n_{out1}}^2} &= -\frac{2}{3} \frac{kT}{C_{S1}} \frac{1}{1 + \frac{g_{m2}}{g_{d3}}} + \frac{kT}{C_{S1}} \frac{1}{g_{d3} \left(\frac{1}{g_{d3}} + \frac{1}{g_{m2}} \right)} \\ &\quad + \frac{2}{3} \frac{kT}{C_{S1}} g_{m4} \left(\frac{1}{g_{d3}} + \frac{1}{g_{m2}} \right) \\ \overline{V_{n_{out2}}^2} &= -\frac{kT}{C_{SC}} \frac{1}{g_{d6} \left(\frac{1}{g_{d6}} + \frac{1}{g_{m7}} \right)} + \frac{2}{3} \frac{kT}{C_{SC}} \frac{1}{1 + \frac{g_{m7}}{g_{d8}}} \\ &\quad + \frac{kT}{C_{SC}} \frac{1}{g_{d8} \left(\frac{1}{g_{d8}} + \frac{1}{g_{m7}} \right)}. \end{aligned} \quad (2)$$

The SNR can be calculated by summing up the noise sources from the three equations. The SNR was measured using 83 samples and plotted as a function of the integration time for three different light powers. Fig. 5 shows a comparison between the calculated and measured SNR, showing the standard error bars for three of the samples. The maximum SNR is around 45 dB, which is a property of the pixel and is achieved at a specific integration time that depends on the power of the incident light. The inset figure shows that the SNR decreases beyond the saturation

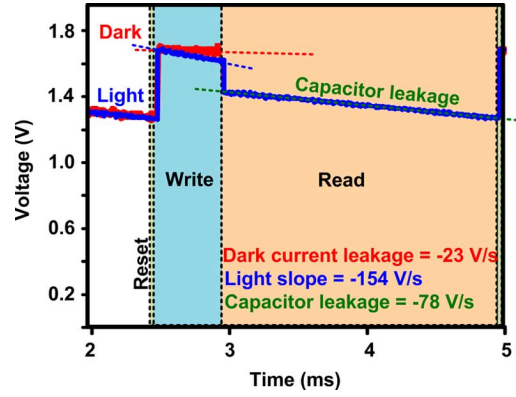


Fig. 6. Measured storage capacitor leakage of the ultrahigh-speed APS.

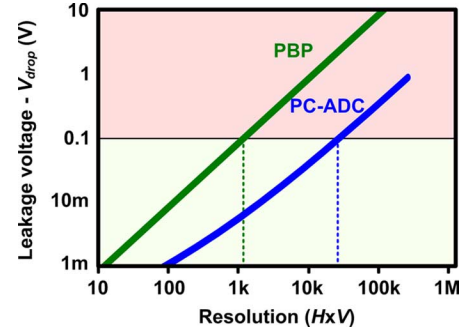


Fig. 7. Simulation results of the maximum leakage from storage capacitor 1 in pixel (0,0), to storage capacitor 8 in pixel (H, V), for *PBP* and *PC-ADC* readout architectures with 8-bit resolution ADCs, four 8-bit parallel outputs and a $\tau_{ADC} = 128$ ns, for a clock rate of 50 MHz ($\tau_{RO} = 20$ ns).

point of the pixel, which happens since the signal no longer increases while the noise increases mainly due to shot noise that is a function of the integration time.

V. DESIGN SCALABILITY

The limitation on the scalability of this design depends on the array readout time since the storage capacitors can leak their charge. The leakage of the storage capacitor was measured by applying a short reset period, followed by a short write period (WT_1 is on), and then turning the write switch off, while keeping the read switch (RD_1) on the whole time. Fig. 6 shows the measured storage capacitor leakage rate, which was -78 V/s.

Fig. 7 shows the maximum leakage based on the FR calculations using the following equations:

$$FR_{PBP} = \left[H \times V \left(\tau_{ADC} + \frac{b}{n} \times \tau_{RO} \right) \right]^{-1} \quad (3)$$

$$FR_{PC-ADC} = \left[H \times V \left(\frac{\tau_{ADC}}{V} + \frac{b}{n} \times \tau_{RO} \right) \right]^{-1} \quad (4)$$

where *PBP* and *PC-ADC* are the pixel-by-pixel and the per-column ADC array readout techniques, respectively. H and V are the number of rows and columns in the array, respectively, τ_{ADC} is the time it takes the ADC to complete one conversion, τ_{RO} is the time it takes the chip I/O to send out the converted digital result, b is the number of digital bits, and n is the number

of parallel outputs. Assuming a 100 mV acceptable drop, using a PBP readout architecture would limit the resolution to an array of roughly 32×32 , whereas, a PC-ADC readout would be limited to an array size of roughly 168×168 .

VI. CONCLUSION

We have demonstrated the feasibility of using *in-situ* frame storage for ultrahigh-speed CMOS imaging. Based on simulation results, the pixel can achieve an electrical image capture rate of 1.25 billion fps, which is reasonable since the transistors used are operated well below their cutoff frequency limit, and in a range where the IBM simulation models are accurate. However, this limit was not achievable experimentally with a regular photodiode due to the high illumination intensity required. The sensor used can achieve a speed of 1 million fps. For higher frame rates, we recommend using a high sensitivity light sensor such as a single photon detector with the pixel. Also, if a large array is needed, low leakage storage elements are necessary. We recommend using low-leakage metal-insulator-metal capacitors; however, the fill-factor will be decreased.

REFERENCES

- [1] M. M. El-Desouki, M. J. Deen, Q. Fang, L. Liu, F. Tse, and D. Armstrong, "CMOS image sensors for high speed applications," *Sensors*, vol. 9, no. 1, pp. 430–444, 2009.
- [2] N. Faramarzpour, M. M. El-Desouki, M. J. Deen, S. Shirani, and Q. Fang, "CMOS photodetector systems for low-level light applications," *J. Mater. Sci.: Mater. Electron.*, vol. 20, pp. 87–93, Jan. 2009.
- [3] A. I. Krymski, D. Van Blerkom, A. Andersson, N. Block, B. Mansoorian, and E. R. Fossum, "A high speed, 500 frames/s, 1024×1024 CMOS active pixel sensor," in *Proc. 1999 Symp. VLSI Circuits*, 1999, pp. 137–138.
- [4] A. I. Krymski, N. E. Bock, N. Tu, D. V. Blerkom, and E. R. Fossum, "A high-speed, 240-frames/s, 4.1-Mpixel CMOS sensor," *IEEE Trans. Electron Devices*, vol. 50, no. 1, pp. 130–135, 2003.
- [5] Y. Nishikawa, S. Kawahito, M. Furuta, and T. Tamura, "A high-speed CMOS image sensor with on-chip parallel image compression circuits," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, 2007, pp. 833–836.
- [6] M. Furuta, T. Inoue, Y. Nishikawa, and S. Kawahito, "A 3500 fps high-speed CMOS image sensor with 12b column-parallel cyclic A/D converters," *Tech. Dig. VLSI Circuits*, pp. 12–22, 2007.
- [7] S. Kleinfelder, S. Lim, X. Liu, and A. El Gamal, "A 10000 frames/s CMOS digital pixel sensor," *IEEE J. Solid-State Circuits*, vol. 36, pp. 2049–2059, Dec. 2001.
- [8] R. Ghannoum and M. Sawan, "A 90 nm CMOS multimode image sensor intended for a visual cortical stimulator," in *Proc. Int. Conf. Microelectronics (ICM)*, 2007, pp. 197–182.
- [9] J. Dubois, D. Ginhac, and M. Paindavoine, "A single-chip 10000 frames/s CMOS sensor with *in-situ* 2D programmable image processing," in *Proc. Int. Workshop on Computer Architecture for Machine Perception and Sensing*, 2006, pp. 124–129.
- [10] N. Stevanovic, M. Hillegrand, B. J. Hostica, and A. Teuner, "A CMOS image sensor for high-speed imaging," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2000, pp. 104–105.
- [11] S. Lauxtermann, P. Schwider, P. Seitz, H. Bloss, J. Ernst, and H. Firla, "A high speed CMOS imager acquiring 5000 frames/sec," *IEDM Tech. Dig.*, pp. 875–878, 1999.
- [12] T. Sugiyama, S. Yoshimura, R. Suzuki, and H. Sumi, "A 1/4-inch QVGA color imaging and 3-D sensing CMOS sensor with analog frame memory," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2002, pp. 434–435.
- [13] T. G. Etoh, D. Poggemann, G. Kreider, H. Mutoh, A. J. P. Theuwissen, A. Ruckelshausen, Y. Kondo, H. Maruno, K. Takubo, H. Soya, K. Takehara, T. Okinaka, and Y. Takano, "An image sensor which captures 100 consecutive frames at 1000000 frames/s," *IEEE Trans. Electron Devices*, vol. 50, no. 1, pp. 144–151, 2003.
- [14] S. Kleinfelder, Y. Chen, K. Kwiatkowski, and A. Shah, "High-speed CMOS image sensor circuits with *in-situ* frame storage," *IEEE Trans. Nucl. Sci.*, vol. 51, pp. 1648–1656, Aug. 2004.
- [15] N. Faramarzpour, M. J. Deen, S. Shirani, and Q. Fang, "Fully integrated single photon avalanche diode detector in standard CMOS 0.18- μm technology," *IEEE Trans. Electron Devices*, vol. 55, pp. 760–767, Mar. 2008.
- [16] M. M. El-Desouki, M. J. Deen, and Q. Fang, "High speed imaging through in-pixel storage, USPTO," U.S. 12814443, Jun. 12, 2010.
- [17] H. Tian, B. Fowler, and A. El Gamal, "Analysis of temporal noise in CMOS photodiode active pixel sensor," *IEEE J. Solid-State Circuits*, vol. 36, pp. 92–101, Jan. 2001.



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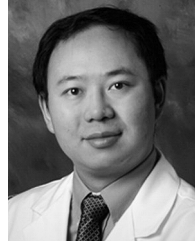
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