CMOS Image Sensors and Camera-on-a-Chip for Low-Light Level Biomedical Applications

M. Jamal Deen, Munir M. El-Desouki and Naser Faramarzpour

Electrical and Computer Engineering Department, McMaster University
1280 Main Street West Hamilton, ON L8S 4K1, Canada
E-mail: jamal@mcmaster.ca

Abstract – **With the advances in deep submicron CMOS technologies, CMOS-based active-pixel sensors (APS) have become a practical alternative to charge-coupled devices (CCD) imaging technology. Key advantages of CMOS image sensors are that they are fabricated in standard CMOS technologies, which allow full integration of the image sensor along with the analog and digital processing and control circuits on the same chip and that they are of low cost. Since there is a practical limit on the minimum pixel size (4~5 μm), then CMOS technology scaling can allow for an increased number of transistors to be integrated into the pixel. Such smart pixels truly show the potential of CMOS technology in imaging applications, especially for high-speed applications. This work discusses various active-pixel sensors (APS) and shows the feasibility of using the DC-level to increase the sensitivity of the pixel for low-level light applications. Avalanche-photodiodes (APDs) are described, in addition to a discussion of the breakdown mechanism and microplasma in avalanche breakdown for single photon APDs. A fully integrated, 16×16 pixel CMOS camera-on-a-chip, fabricated in a standard CMOS 0.18 μm technology is also shown in this work. The array is based on 256 APS with a pixel size of 20 μm × 30 μm, a fill-factor of 60% with all digital and analog blocks implemented on-chip.**

I. INTRODUCTION

Emerging optical molecular imaging systems have had a revolutionary impact on medicine, biodefense and environmental testing through techniques such as DNA sequencing, protein detection, and evaluation of animal models of human cancer. These techniques are even more attractive when developed in hand-held, light-weight portable devices. The most sensitive optical detection system in use is the photomultiplier tube (PMT). However; PMTs are costly and require high operating voltages, precluding their use in hand-held systems. Furthermore, multiplexed imaging is not feasible using PMTs as they are relatively large and thus unsuitable for dense arrays [1, 2]. Two alternative image sensors that can be used for optical molecular imaging systems are charge-coupled

devices (CCDs) and CMOS imagers. CCDs must remain cooled in order to increase their sensitivity to low-level light for biomedical applications. Also, CMOS image sensors consume less power, operate at higher speeds, and offer much higher levels of integration. The advances in deep submicron CMOS technologies have made CMOS image sensors a practical alternative to the long dominating CCD imaging technology. One of the main advantages of CMOS image sensors is that they are fabricated in standard CMOS technologies, which allow full integration of the image sensor along with the processing and control circuits on the same chip at a low cost.
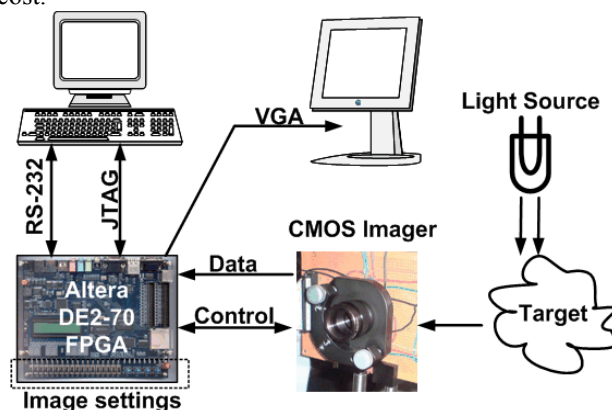

Fig. 1. Block diagram of the CMOS imager setup.

A CMOS camera-on-chip system leads to reduction in power consumption, cost and sensor size and allows for integration of new sensor functionalities. Since there is a practical limit on the minimum pixel size (4~5 μm), then CMOS technology scaling can allow for an increased number of transistors to be integrated into the pixel. For example, when using a CMOS 0.18 μm technology with a 5 μm × 5 μm pixel and a 30% fill-factor (FF), 8 analog transistors or 32 digital transistors can be integrated within the pixel. Since digital transistors benefit more from CMOS scaling properties, digital pixel sensors (DPS) have become very attractive. A DPS integrates an ADC in each pixel, resulting in massively parallel readout and conversion that can allow very high speed operation, where digital data is read out of each pixel. The low FF of
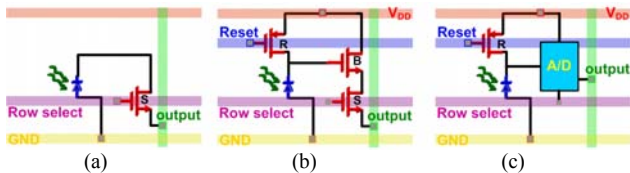
Fig. 2. Passive pixel sensor, (b) three transistor active pixel sensor and (c) digital pixel sensor, with internal analog to digital conversion.

DPS sensors is no longer an issue for CMOS technologies of 0.18 μm and below. The high speed readout makes CMOS image sensors suitable for very high-resolution imagers (multi-megapixels) particularly video applications. In [3], a 352 × 288 pixel CMOS image sensor that is capable of operating at 10,000 frames/s (1 Gpixel/s) with a power consumption of 50 mW is presented.

Fig. 1 shows a block diagram of the CMOS imager setup, where the CMOS imager is controlled by the FPGA board through the expansion slot and the image settings, such as integration time, averaging or correlated-double sampling, could be adjusted by the switches on the board. The FPGA board is also in charge of interfacing to the VGA monitor to display the captured images in video mode, as well as interfacing to the PC to upload the captured images through the RS-232 link for further processing.

In this work, we discuss various APS designs and show the feasibility of using the DC-level of the APS output to increase the pixel's sensitivity for low-light-level applications. Next, APDs are described and the breakdown mechanism and microplasma in avalanche breakdown for single photon APDs are discussed. Next, a fully integrated, 16 × 16 pixel CMOS camera-on-chip, fabricated in a standard CMOS 0.18 μm technology is presented. The array is based on 256 active-pixel sensors with a pixel size of 20 μm × 30 μm, a fill-factor of 60% and a total array area of 646 μm × 390 μm. All digital and analog blocks, including the row and column controllers, multiplexing circuits, sample-and-hold circuit and dual-slope analog-to-digital converter (ADC), have been implemented on-chip. The imager was tested by controlling it with an Altera DE2-70 FPGA board. When clocking the ADC at a frequency of 1 MHz, images were captured at 60 frames/s. Finally, the conclusions are presented.

II. DIFFERENT PIXEL STRUCTURES

Different pixel structures have been reported for CMOS imagers. Each pixel structure has its advantages and can be suitable for specific applications. In the following sub-sections, some common CMOS pixel structures will be presented, and their applicability to low-light-level applications will be discussed.

A. Passive-, Active- and Digital-Pixel Sensors

Passive pixel sensor (PPS) is the earliest and most simple CMOS pixel structure. In PPS, each pixel consists of a photodiode and a row-select transistor. Fig. 2a shows the PPS structure. The PPS has only one transistor per pixel, and thus it has the highest FF. However, column readout of the rather small integrated charge of the photodiodes significantly reduces the performance of this approach.

The active pixel sensor (APS) is the most popular CMOS pixel structure. The three-transistor APS circuit is shown in Fig. 2b. In this structure, the reset is done internally. The sense node is isolated from the readout column by using a source follower. Compared to PPS, this structure has better signal-to-noise ratio (SNR). Individual circuitry in each pixel, however, increases the non-uniformity of the pixels outputs under same illumination levels (known as fixed-pattern noise, FPN). A large part of FPN is due to the variation of the sense node voltage after reset, which is known as reset noise. Correlated double sampling (CDS) can be used to remove this noise. In CDS, every pixel's output is read twice.

The most recent CMOS pixel structure is DPS, shown in Fig. 2c. In this pixel structure, the AD conversion of the signal is done partially inside the pixel, so that the output of the pixel is digital. DPS is a great solution for integrated and high speed digital imaging. It however has a low fill-factor, and it suffers from the inherent quantization noise due to the AD conversion, which limits its applicability in ultra-sensitive measurements.

B. DC Level Mode APS

Active pixel sensors, in general, have an output with low signal-to-noise ratio (SNR) for low-levels of light. One way to increase the sensitivity of the APS is to increase its photodiode's size. This solution, however, will decrease the resolution of the imager. Another solution is to lengthen the integration time of the APS. The pixel is capable of detecting lower levels of light with longer integration times. However, the rate of spatial variation of the sample can limit the applicability of this solution. Also, at long integration times, the internal dark current of the pixel may saturate it.

Fig. 3 shows the simulated sense node voltage of the APS circuit, shown in Fig. 2b. Fig. 3 shows several reset and integration cycles of the sense node voltage, simulated for three levels of photocurrent. The voltage drop during integration, which is shown in Fig. 3 as swing output, is proportional to the power of incident light. This is expected, as for higher levels of light, the photocurrent is higher and discharge of the capacitance of the photodiode happens faster. Interestingly, Fig. 3 also shows that the DC level of the sense node voltage varies with light. This is mainly due to the incomplete reset of the photodiode, during the short integration time. Fig. 4 shows the measured and calculated SNR of the pixel. The SNR values have been evaluated by multiple measurements of the signal at each level of light input. About 50 to 100 voltage samples are collected at each illumination level, their mean is interpreted as the signal value, and their standard deviation as the noise. The SNR has been evaluated for both swing ($v_2 - v_1$) and DC level ($v_2 + v_1$)/2. The chip is illuminated at 640 nm using a narrowband filter ($\Delta\lambda \approx 20$ nm). The light power is measured with a Newport calibrated power meter at the same wavelength. Our low levels of light power are achieved by using several attenuators in the optical path. At light powers less than 0.1 μW/cm^2, the measured power by the power meter is very noisy compared to the DC level of our pixel, which is still very stable. At these low levels of light, the output of the power meter has been sampled multiple times, and then averaged to provide the light power values shown.
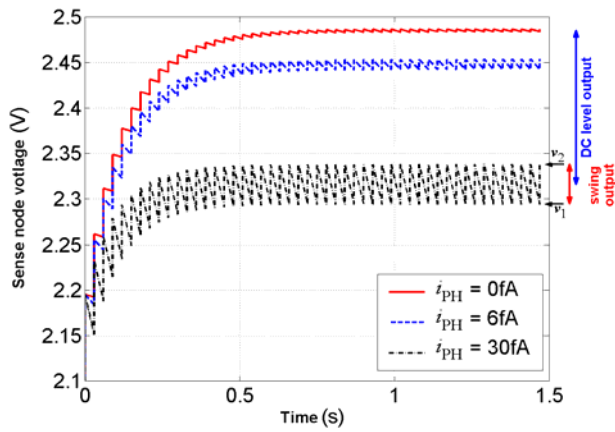
Fig. 3. Total sense-node voltage versus time for different levels of photocurrent corresponding to different low-level light illumination conditions. In the absence of photocurrent, the swing output is due to the internal dark current of the photodiode. Note that the DC level varies more than the swing, for the same level of incident light [4].
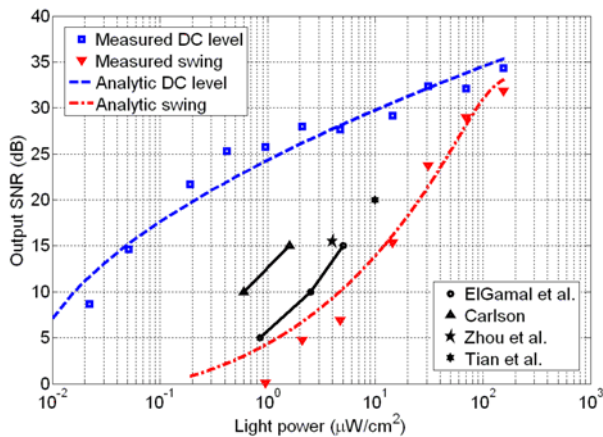

Fig. 4. Analytically calculated SNR of the APS, measured SNR values for our APS, and SNR values reported for some other low light level APS circuits in the literature (from the top: [5], [6], [7], [8]). The data has been gathered from a variety of pixel sizes. The size of the pixels used in the experiments affects the reported SNR values at different light powers. The data have been adjusted to compensate for the size differences and to make a fair comparison of the different reported SNR values. [4]

Measurement results in Fig. 4 show that the DC level of the output can detect light levels which are two decades or less compared to the swing of the same pixel. The DC level has about 20 dB better signal-to-noise ratio than the swing at about 1 μW/cm². The DC level output has also been compared to some SNR values of other APS circuits reported in literature. Fig. 4 shows some SNR points achieved in the work of El Gamal *et al.* [5], Carlson [6], Zhou *et al.* [7], and Tian *et al.* [8]. It should be noted that parameters like the pixel size, integration time or readout rate, or the illumination spectrum affect the SNR of the APS, and they should be considered to make a fair comparison of the performance of the pixels. Appropriate changes have been made to the SNR points in Fig. 4 to account for these differences. For example, the integration times of the pixels were 30 ms in all works except in [6] which was 8 ms, for which a 3 dB correction was made to the SNR value. For the light power at the low levels of Fig. 4, the SNR of the DC level stands well above the conventional APS.

C. Pixels with Avalanche Photodiode

All of the above pixel structures operate by integrating the photocurrent. In applications where the signal is changing very fast, short integration times are necessary to obtain the desired temporal resolution. However, detection of lower levels of light requires the small photocurrent to be integrated during longer integration times. These approaches cannot serve the applications that require sensitivity and fast response at the same time. APDs operated in Geiger mode, are the semiconductor equivalent of PMTs. Geiger mode APDs are capable of detecting single photons.
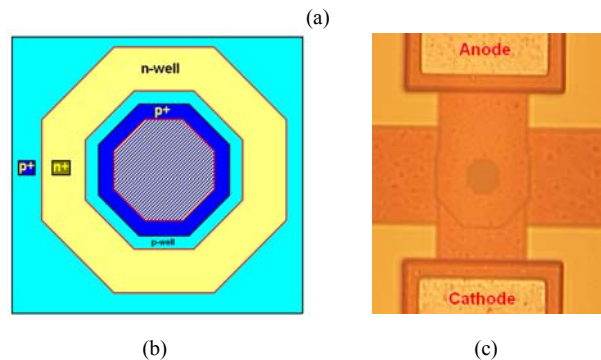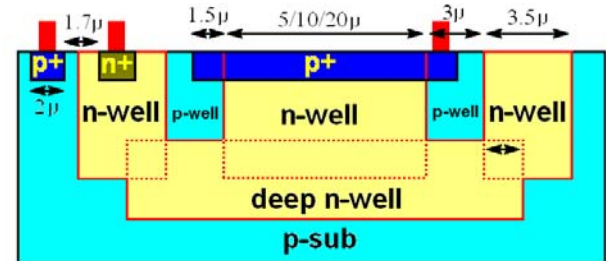

(a)

(b)   (c)

Fig. 5. (a) Cross section and (b) plan view of the layout of our APD. Putting an n-well, inside a p⁺ region creates the avalanche area and also the guard ring. (c) The photomicrograph of the APD device layout with a 10 μm diameter. [4]
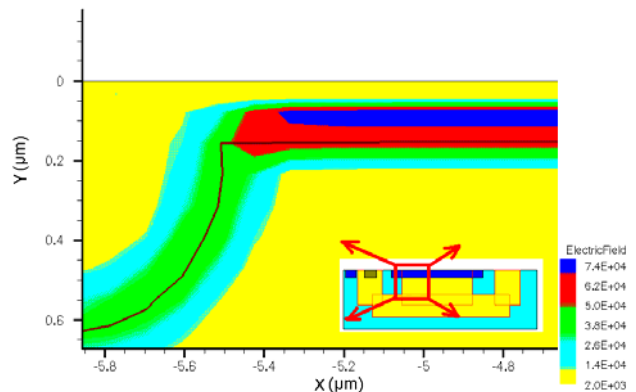

Fig. 6. Device simulation of the APD under reverse bias, using the DESSIS tool. It shows that the maximum electric field will appear in the desired p⁺/n-well junction [4].

A regular p⁺/n-well diode was fabricated in standard CMOS technology as a p⁺ region implanted within an n-well region. In this diode, the breakdown current will not flow uniformly across the area of the p⁺ region. The breakdown region of such diode will be at its edge. This is due to the higher peak electric field caused by the narrower depletion region at the corners of the diode junction. As the reverse bias increases, the electric field at the perimeter

will reach the onset of avalanche first, and the current will flow there. However, in APDs, the breakdown region should be spread over the area of the diode and not at its corners. We have made this possible by creating a p-type guard ring around the p$^+$ active area of the APD, as shown in Fig. 5. To create the guard ring, an n-well region is placed within the p$^+$ region, which is against the conventional design rules of the standard CMOS. In our design, the width of the guard ring is 3 μm, with a depth of approximately 0.5 μm. The doping concentration of the p-well is in the range of 10^{17} cm^{-3}, compared to 10^{19} cm^{-3} for the p$^+$ region. It will be shown that the designed device has excellent avalanche characteristics. However, it should be noted that standard CMOS technology is targeted for digital and analog applications and not optical imaging devices. Most of our design parameters are not optimum, and are dictated by constraints of the fabrication technology. But because it is a standard technology, the cost is very low. Fig. 5c shows the photomicrograph of the APD device layout with a 10 μm diameter fabricated in a standard 0.18 μm, single poly, six metal, salicide CMOS technology. Design rules of the technology do not allow circular features. We have used 45° rotated lines to draw octagons, the closest shape that can be generated to circles.

Fig. 6 shows the profile of the electric field created in our APD. The GENESIS simulation package was used to simulate some of the APD performance characteristics. The structure is produced with MDRAW, and the electric field profile is obtained with DESSIS. Fig. 6 shows that the peak electric field is spread under the active region of the APD, which is the p$^+$/n-well junction.

III. APD Breakdown and Microplasma

The APD layout ensures that the maximum electric field happens across the active area of the APD, rather than at its edges or corners. Impact ionization requires an electric field of at least E_m = 300 kV/cm [9]. In a reverse-biased diode, the peak is located at the metallurgic junction. When the reverse bias is just above the breakdown voltage, a narrow strip of high electric field region around the metallurgic junction is where impact ionization occurs, rather than in the entire depletion region.

The high electric field region of Fig. 7 can be only a few atoms wide. In this narrow region, any device imperfection can cause a local disturbance of the electrical field that can lead to a reduction of the breakdown voltage to a value below the breakdown voltage of the surrounding uniform junction. These tiny spots will be the site of the localized avalanche breakdown of the device. This breakdown condition is generally regarded as being a solid-state analogy of gas discharge plasma, and it is called microplasma. The microplasma can occur at threading dislocations, metal-rich precipitates, diffusion induced stacking faults, dopant impurity dislocations, diffusion voids and cracks or mechanical damage.

At the onset of avalanching, microplasmas switch on and off randomly, producing current pulses of constant height. The microplasma is on for an increasing fraction of the time as the voltage increases until it becomes quiescent. The current carried by microplasma is limited by heating, spreading resistance and space charge effects.
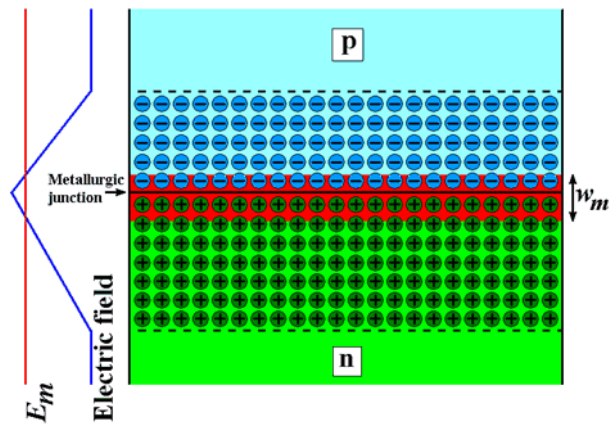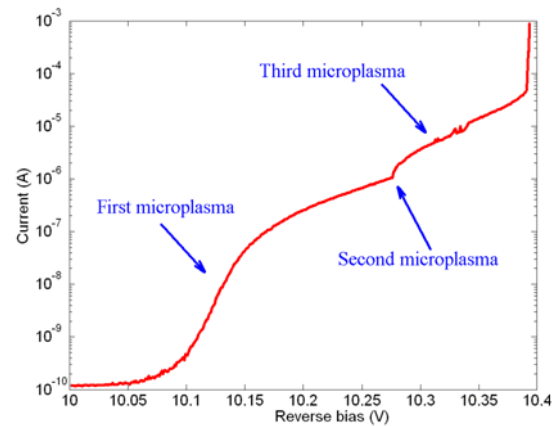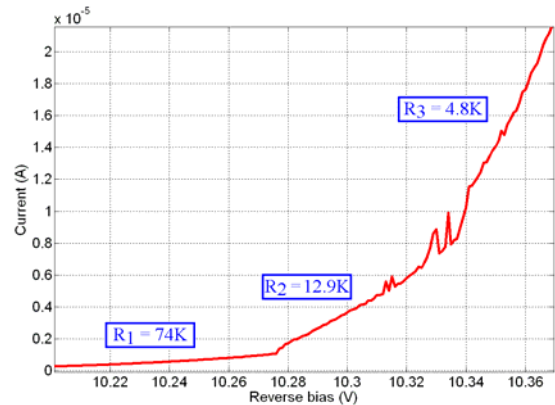

Fig. 7. Schematic of an abrupt p/n-junction at avalanche breakdown. The width of part of the depletion region with an electric field high enough for impact ionization, w_m, is only a small fraction of the total width of the junction depletion region [4].

(a)

(b)

Fig. 8. (a) Measured *I-V* curve of one of our 10 μm APDs at the onset of breakdown (multiplication region, where the current is multiplied by a finite *M*). The curve shows that the current increases in steps, before complete breakdown. (b) A zoomed version of (a) drawn in linear scale. Different sections of the current curve have resistive characteristics. It can also be seen that the third microplasma turns on and off a few times before being permanently on. [4]

Fig.8 shows the microplasma occurrence in one of our APDs. The I-V curves are obtained by a semiconductor parameter analyzer, with a 1 kΩ resistor in series with the APD. Fig. 8a shows the I-V curve of the APD in semi-log scale. At about 10.05 V, the avalanche multiplication starts and the reverse current of the APD increases. The increase however, does not sharply continue beyond 10.15 V, as it
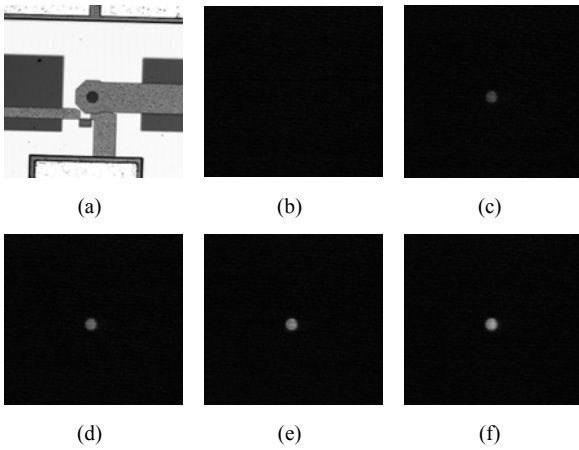
Fig. 9. Photomicrograph of the APD circuit, with the microscope light on. The circuit consists of a 10 μm APD with a 100 kΩ resistor in series. The APD has a measured 10.2 V breakdown voltage. Photomicrographs taken with the microscope light off, for a reverse bias of (b) 19 V, (c) 20 V, (d) 21 V, (e) 22 V and (f) 23 V. [4]
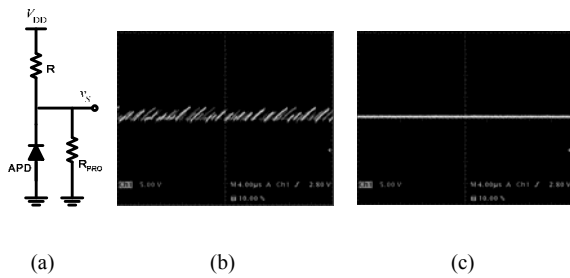

Fig. 10. The APD circuit (a) and its measured signal, v_S, at (b) 19 V and (c) 20 V applied V_{DD}. The series resistor R = 100 kΩ and the probe resistor R_{PROBE} = 1 MΩ. [4]
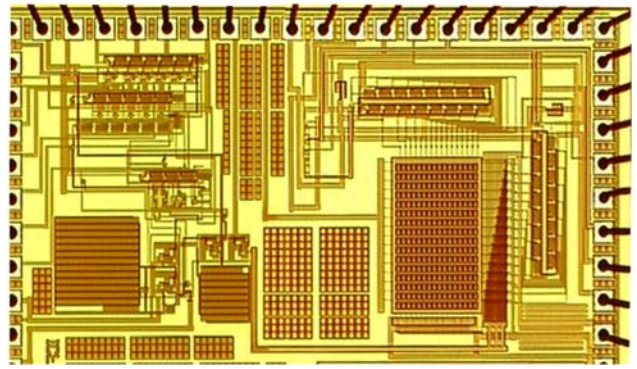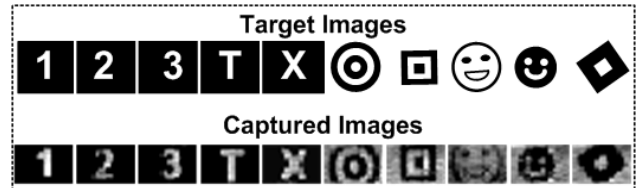

Fig. 11. CMOS camera-on-a-chip layout photomicrograph.

Fig. 12. Target images (resized for comparison) compared to the non-processed captured images shown in their original resolution of 256 pixel.

seems to saturate. This saturation in semi-log scale is in fact a linear relationship, or a resistive characteristic, meaning that the microplasma tube is acting like a resistance. The resistance is calculated in the linear scale of Fig. 8b to be R1 ≈ 74 kΩ. At above 10.28 V, a second microplasma tube is turned on. The microplasma tubes will now perform like two resistors in parallel, with the resistance of the second microplasma R2 ≈ 12.9 kΩ. At around 10.31 V, the third microplasma becomes active. As it was mentioned before, a microplasma tube can turn on and off at the onset of avalanche. This can be seen in Fig. 8b. The resistance of the third parallel microplasma is calculated to be around R3 ≈ 4.8 kΩ. At 10.4 V, so many microplasma tubes are on that the APD can generate currents more than 1 mA.

It is reported that APDs emit light from the microplasma sites during breakdown [10]. We have examined this fact by looking at an APD during breakdown in the dark. Fig. 9a shows a photomicrograph of an integrated 10 μm APD in series with a 100 kΩ resistor, with the circuit schematic shown in Fig. 10a. Fig. 9 shows several photos taken from the same spot on the chip at dark. When the applied voltage, V_{DD}, is gradually increased, the APD starts to emit light at 19.3 V. When the applied voltage is decreased from a level higher than 20 V, the APD stops emitting light at 19.1 V. Fig. 10 also shows the APD voltage, v_S, captured on the oscilloscope screen. Fig. 10b is taken at 19 V bias, where the APD is working in Geiger mode, which is used for single photon detection. Fig. 10c shows the APD signal at 20 V, where the APD is constantly on, and emits light. The APD current in Fig. 10c

is measured to be about 80 μA. When the applied voltage is increased above 20 V, the light emission from the APD increases, as shown in Fig. 9. The voltage across the APD also increases, from about 10.5 V at 20 V, to about 11.5 V at 23 V supply. This series resistance in sustaining breakdown condition is known to be R_S [9], and is considered an effect of space charge, Ohmic drops and local heating. In this example, R_S is approximately 50 kΩ.

IV. CMOS IMAGER DESIGN

Fig. 11 shows the layout photomicrograph of the complete camera-on-a-chip fabricated in a standard CMOS 0.18 μm technology, which occupies an area of 3 mm × 1.5 mm. A standard 3-transistor APS, similar to the one shown in Fig. 2b, was used, where the reset transistor is a PMOS device. Although the PMOS device will reduce the fill-factor (FF) due to the need for an extra well, it allows for a higher dynamic-range of full supply (1.8 V). The photodiode was implemented as an n+/p-substrate diode for maximum sensitivity. Both the common source buffer and output row-selection device are NMOS transistors. All transistors are of minimum feature size to maximize the FF, which was 60% in this case. The actual layout area of the pixel was 20 μm × 30 μm. Only the photosensitive area of the photodiodes is exposed in the array, and everything else is covered with the top metal layer.

In this camera-on-a-chip, the row and column scanners were used instead of decoder circuits in order to reduce the control lines coming into the chip. Also, only one input clock is needed to control the row and column circuitry. The multiplexed output is buffered by an on-chip op-amp, which provides the chip's analog output that is only used for testing and comparison purposes. The analog voltage is routed to the sample-and-hold (S/H) circuit and ADC. The ADC used was a 6-bit dual-slope integrating topology clocked with a 1 MHz clock that was provided by the FPGA. A maximum of 64 clock-cycles is required to complete the conversion, which results in a frame-rate of

60 frames/s. The chip provides both parallel and serial outputs from the ADC for testing purposes. A large capacitor was used in the S/H circuit to reduce charge-injection effects. All elements, including the state-machine, counters and buffers were implemented on chip.

The CMOS imager was tested on an optical table with a 25 mm diameter achromat lens that has an effective focal length of 15 mm. The Altera DE2-70 FPGA board was used for controlling the CMOS imager and all of the FPGA code was written in Verilog. The tested targets were kept 44 cm away from the imager and had a height of about 2 cm. Fig. 12 shows some examples of the captured images that were uploaded to the PC using the RS-232 link in the FPGA. The images shown are not processed or averaged, nor was correlated-double sampling used.

IV. CONCLUSION

This paper demonstrates the great potential of CMOS technology to be used in biomedical imaging applications. The DC level APS is an excellent choice for low-level light applications. It uses the same pixel structure as the APS. The speed of APS-based structures are however limited, due to the fact that they integrate the photocurrent. For applications that require both sensitivity and fast response, APDs should be selected. The APDs with active peripheral circuitry offer the highest speed at the cost of larger pixel sizes. However, by incorporating the advantage of small transistor sizes of modern CMOS technologies, APDs with peripheral circuitry become an excellent choice for achieving both high speed and high sensitivity performance. Also, single photon APD operation was described, including the occurrence of microplasma in avalanche breakdown. Microplasma sites are bistable below their saturation currents, and this is the regime where APD can be used in Geiger mode. Above the saturation current level, however, microplasma are self-sustaining and photoelectron multiplication is reduced, but the microplasmas emit light. The paper also describes a fully integrated 256-pixel CMOS camera-on-a-chip fabricated in a standard CMOS 0.18 μm technology.

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